Research on Design Scheme of Adjustable Numerical Control Three-Phase Power Supply

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Abstract. This paper introduces a design scheme of adjustable digital controlled three-phase power supply based on single chip microcomputer. It takes FPGA and single chip microcomputer as the main control core, using DDS technology to realize the occurrence of the waveform and control, which increases the intuitive use of the power supply through the LCD display circuit and the power supply is convenient to operate with keying circuit.

Introduction

Direct digital synthesizer (DDS) is a new frequency synthesis technology developed in recent years [1], It can realize the high stability, high precision and high resolution of the output waveform. The development of programmable logic device (FPGA, CPLD, etc.) provides a better technical means for the realization of DDS [2], and it is very suitable for implementing the digital circuit part of the waveform.

The Design of System Overall Scheme

This design is based on FPGA, single chip microcomputer as the main control core, which controls the input of the keyboard and LCD displaying, and completes the data transmission between the single chip microcomputer and FPGA. FPGA outputs the address to the memory, so that it transfers the data of the corresponding unit to the D / A converter, and then through the adjustable band pass filter for waveform shaping and power amplifier, finally transformer conveys the complete three-phase electrical signal. It can output sine wave, also can output arbitrary waveform signal. The frequency range is from 30Hz to 70Hz and from 350Hz to 450Hz output by three-phase voltage signal, the phase is in the range of 0 to 360 °, step 0.1 ° adjustable, output frequency step 0.01Hz adjustable. Fig. 1 is the scheme diagram of system.

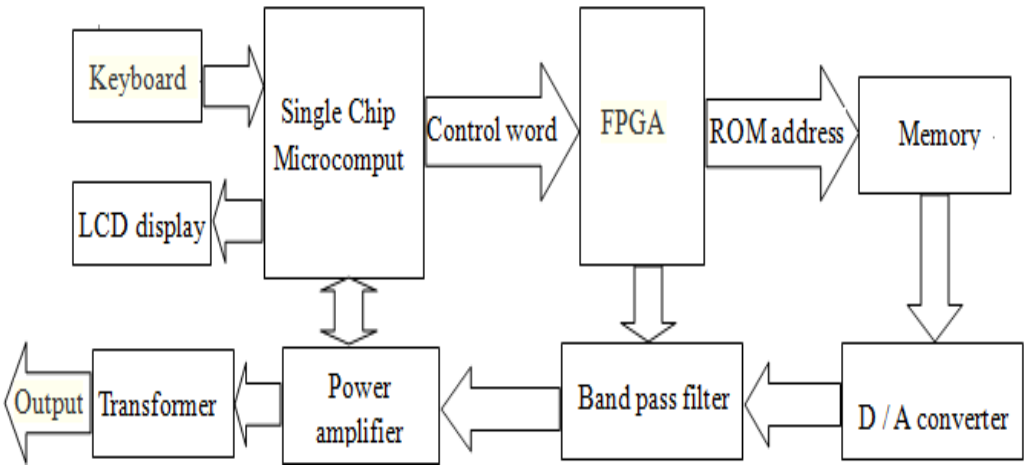

Figure 1. The scheme diagram of system

The Implementation of the Core Modules

The scheme is mainly composed of single chip microcomputer, FPGA, band pass filter, power amplifier and transformer. The following will introduce the implementation plan of system's core part.

The Implementation Plan of DDS. This plan is using DDS technology to achieve the occurrence of the waveform and control, It produces sine wave which frequency and phase can be controlled mainly based on the numerical control oscillator , its essence is to control the equal interval sampling for the phase [3].

Phase accumulator is the core of DDS, It consists of an N-bit word-length adder and an N-bit phase register sampled by a fixed clock pulse [4]. When the DDS is operating normally, under the control of the standard reference frequency source, the phase accumulator continuously performs phase linear accumulation(each time the cumulative value is frequency control word K), it will produce a overflow to complete a cyclical action when the phase accumulator is full, this cycle is the frequency cycle of the DDS synthesis signal [5]. Eq. 1 is the frequency of the output signal.

$$f_{out} = \frac{w}{2\pi} = \frac{\frac{2\pi}{2^N} \times K \times f_c}{2\pi} = \frac{K \times f_c}{2^N}. \quad (1)$$

It is obvious that the output frequency is minimum when K=1,the frequency resolution is $f_{min} = \frac{f_c}{2^N}$ .f_{out} is the frequency of output signal; K is the frequency control word; N is the word length of the phase accumulator; f_c is the working frequency as standard of reference frequency source.

In this scheme, the adjustable precision of required phase is 0.1° , the adjustable precision of frequency will reach 0.01Hz. Since a cycle is 360 °,so it take sampling of 3600 points in a period. In order to facilitate the calculation and improve the accuracy, the choice of clock frequency is 18 MHz. Eq. 2 is the maximum count of the phase accumulator. Eq. 3 is the minimum number of N for the phase accumulator.

$$P_{acc} = \frac{f_c}{f_{min}} = \frac{3.6 \times 10^6 Hz}{0.01Hz} = 3.6 \times 10^8 \quad (2)$$

$$N = \left\lceil \frac{\lg(Pacc)}{\lg 2} \right\rceil = \left\lceil \frac{\lg(3.6 \times 10^8)}{\lg 2} \right\rceil = 29 \quad (3)$$

Because the frequency is 3.6×10^6Hz, the cumulative number of phase accumulator in a cycle is 3.6×10^8 and the number of times for sampling are 3600, so Eq.4 is the count value for sampling at one time as required.

$$n = \frac{Pacc}{3600} = \frac{3.6 \times 10^8}{3600} = 10^5 \quad (4)$$

The calculation method of bit width input by frequency word is as follows: the frequency resolution is 0.01Hz,the highest frequency is 70Hz,then there are: 70/0.01=7000, the input of frequency word is 13 bits; the highest frequency is 420Hz, then there are: 420/0.01=42000, the input of frequency word is 16 bits.

The calculation method of bit width input by phase word is as follows,the phase resolution is 0.1 degrees, then there are: 360/0.1=3600, the input of phase word is 12 bits.

The Implementation Scheme of Mutation Signal Output by Three Phase Voltage. Divide the storage space of external memory into two workspaces or a number of storage space, The normal signal ROM unit and mutation signal storage space, that is ROM unit of the normal signal and the storage space of mutation signal, the address data can be added to the fixed offset to realize the occurrence of the mutation signal when the mutation signal is selected to output [6]. Fig. 2 is the assignment scheme of ROM lookup table address.

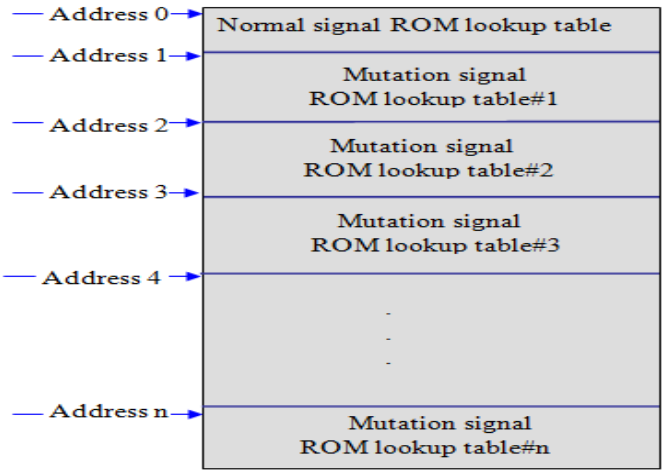

Figure 2. The assignment scheme of ROM lookup table address

The Implementation Scheme of Filtering. The scheme requires that the frequency range of system output are two frequency bands ,they are 30Hz to 70Hz and 350 Hz to 450 Hz. Consider here using the bandpass filter to achieve filtering requirements. It is proposed to use the integrated chip MAX264 and which combine with the single chip microcomputer to form a programmable bandpass filter. MAX264 integrates resistance and capacitance which are required for the design of filter, so it is almost no external devices in the application [7,8], this filter can achieve three filtering methods through the choice of working mode,they are lowpass,highpass and bandpass, the cut-off frequency can be sent through the program ,so it is very simple to use.

The Selection of Power Amplifier. The scheme plan to use the highfidelity D class digital power amplifier which is produced by NS Corporation of America as the power amplifier for the output signal of DDS [9,10]. This kind of power amplifier adopts switch technology and new integrated process, the efficiency can reach more than 85%. It has overvoltage, under voltage, overload, short circuit and other perfect protection function.

Conclusion

The signal source designed by this scheme will combine organically the technology of single chip microcomputer, FPGA, DDS and so on and make full use of their respective advantages. The adjustable numerical control three phase power supply realized by the scheme has the advantages of simple method and high Cost performance and high frequency resolution generated by waveform.

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