L/S-Band 0.18 μm CMOS 6-bit Digital Phase Shifter Design

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Abstract. A L/S band 6-bit phase shifter for phased array radar system is designed based on SMIC 0.18*um* standard CMOS process in this paper. The reasonable parameters calculation and optimization are carried out, the circuits layout design is completed, and the phase RMS error of phase shifter is less than 2 °, the insertion loss is less than 2dB, and the layout size is $2.87\times1.2\,mm^2$.

Introduction

Phase shifters and switch circuits are widely used in radar systems, communication systems, microwave devices and measurement systems. The mainly application is for phased array radar [1]. The active phased array antenna is the key to realize the active phased array radar. The T/R (Transmit/Receive) module is the core of the antenna. Typically, there are hundreds or thousands of T/R modules on phased-array antennas, each one can achieve signal transmission.

Fig. 1 shows a block diagram of a typical T/R module. The phase shifter is located at the front end of the T/R module in the phased array radar system. It is a device that can achieve the beam scanning and control the phase change of the signal. Phase shifter is divided into digital and analog. Due to the higher stability, digital phase shifters have a wider range of applications. There are switch-linear, load-linear, reflective and switch-network types which are commonly used. Digital phase shifters are the key elements of T/R module in phased array radar system. The accuracy of radar scanning depends on the bits and accuracy of phase shifter.

In this paper, a 6-bit digital phase shifter cover L/S band (1-4GHz) is designed based on SMIC 0.18*um* CMOS process. The detailed design principle, circuit topology, theoretical analysis and experimental simulation results are as follows.

Circuit Design

CMOS switch has the advantages of simple control circuit and low power consumption [2]. By controlling the gate bias voltage of the switch, it is switched between the reference state and the phase-shifted state to obtain the desired phase shift [3]. Typically, a large resistor (usually not less than $20\,K\Omega$) is connected to the gate of the MOS transistor to prevent signal leakage and oxide breakdown. In the on-state, the MOS transistor is equivalent to a resistor; in the off -state, it is equivalent to a capacitor. The gate bias voltage and the width of the MOS transistor will affect the performance of the switch [4], thus affecting the accuracy of the phase shift. The selected phase shifter switch on-state voltage is 1.8V, while the cut-off voltage is 0V.

In order to reduce the insertion loss of the switch-network phase shifter, the grounded substrate is compared with the substrate which is connected to the source [5]. When the substrate is grounded, the insertion loss is coupled to the ground from source and drain nodes by the source-substrate

capacitance C_{sb} and the drain-substrate capacitance C_{db}. When the substrate is connected to the source, the source and drain nodes are connected directly through the drain-to-substrate capacitance C_{db}, reducing the isolation between the two nodes. Therefore the substrate that connected to the source is a better choice [6].

The digital phase shifter designed in this paper employs switch-network structure, because the high-low-pass network can realize the flat phase shift in wide frequency band. Broadband phase shifter can be achieved by increasing the order of the filters [7].

Achieving small phase shift steps for 5.625 °, 11.25 °and 22.5 °circuits in a wide frequency range employ the topology of Fig. 2. The inductance in the series band pass network is smaller than that of the parallel band pass network, the area of the circuit can be also saved. In this configuration, the series LC section is used to compensate the phase variations of the low-pass section. To obtain the equations for calculating the optimum component values, the S parameters of the networks were calculated using the transmission matrix parameters.

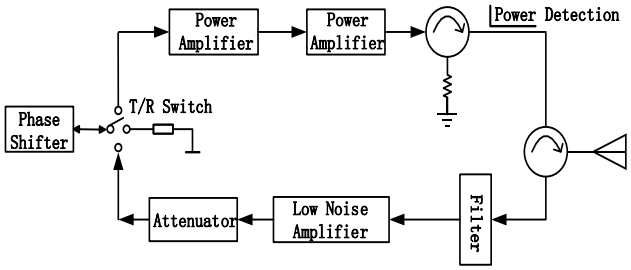

Figure 1. Typical T / R module

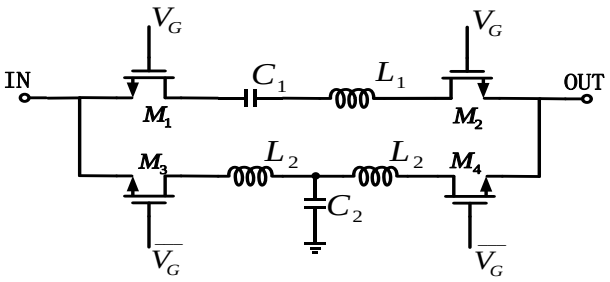

Figure 2. 5.625 °, 11.25 °and 22.5 °phase shift circuit

For low-pass T network, the scattering parameters can be expressed with the following equations:

$$S_{11} = \frac{j\left(2\omega L_2 - \omega^3 L_2^2 C_2 - \omega Z_0^2 C_2\right)}{2Z_0\left(1-\omega^2 L_2 C_2\right) + j\left(2\omega L_2 - \omega^3 L_2^2 C_2 + \omega Z_0^2 C_2\right)} \tag{1}$$

$$S_{21} = \frac{2Z_0}{2Z_0\left(1-\omega^2 L_2 C_2\right) + j\left(2\omega L_2 - \omega^3 L_2^2 C_2 + \omega Z_0^2 C_2\right)} \tag{1}$$

Where Z_0 is the characteristic impedance. At the center frequency, the input is matched, so S_{11} =0. The capacitance C_2 and phase shift are:

$$C_2 = \frac{2L_2}{\omega_0^2 L_2^2 + Z_0^2}, \Delta\phi = -\tan^{-1}\left(\frac{2\omega_0 L_2 - \omega_0^3 L_2^2 C_2 + \omega_0 Z_0^2 C_2}{2Z_0\left(1-\omega_0^2 L_2 C_2\right)}\right) \tag{2}$$

In the band-pass network, the inductor resonates with the capacitor. The phase slope of the low-pass network at the center frequency should be the same as that of the band-pass network in order to achieve better phase performance over the entire bandwidth. The parameter values of the low-pass and band-pass networks are:

$$L_2 = \frac{Z_0 \tan(\Delta\phi/2)}{\omega_0}, C_2 = \frac{\sin(\Delta\phi)}{\omega_0 Z_0}, L_1 = \frac{2Z_0 \tan(\Delta\phi/2)}{\omega_0}, C_1 = \frac{1}{2\omega_0 Z_0 \tan(\Delta\phi/2)} \quad (4)$$

T-type networks have higher phase accuracy and lower group delay compared to π -type networks [8]. Thus 45 °and 90 °phase shift circuits employ the bridge T-type network structure. Fig. 3 shows the bridge T-type network structure and its equivalent circuit. In this topology, the signal path is switched between the low-pass and band-pass networks. The 90 ° circuit is a little different from the 45 °circuit. A capacitor is connected in parallel across the MOS transistor in the 90 °circuit in order to get lower phase amplitude error by reducing the size of the MOS transistor.

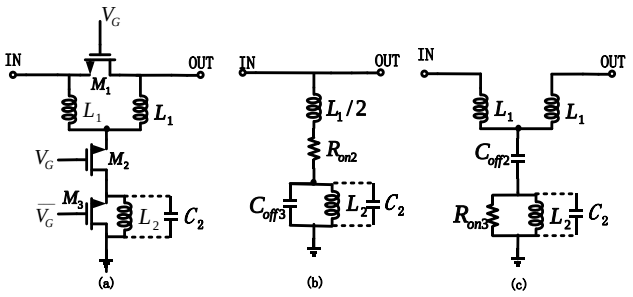

Figure 3. 45 °and 90 °phase shift circuit

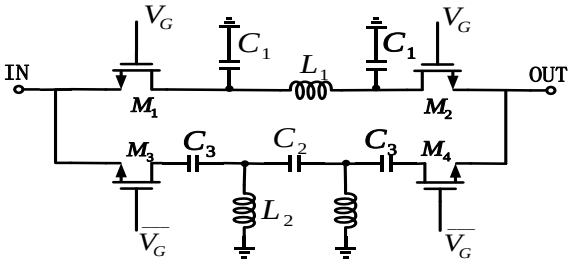

Figure 4. 180 °phase shift circuit

In one state, when the gate bias control voltage is high, the transistor M_1 and M_2 are turned on, and M_3 is turned off. The circuit is equivalent to the circuit of Fig. 3(b). There is a cut-off capacitor due to parasitic effects of the M_3 transistor in the non-ideal case. This configuration provides zero phase shift at the center frequency. The inductor L_2 is designed to resonate with the capacitor C_{off3}.

In the other state, when the control voltage is low, the transistors M_1 and M_2 are turned off, and M_3 is turned on. The equivalent circuit is shown in Fig. 3(c), at the center frequency of operation, the low-pass filter is designed to exhibit the desired phase shift. And its phase frequency slope is equal to the phase frequency slope of the zero phase shift network. Compared with other topologies, this structure has lower insertion loss because it has only one series switch in the RF signal path. The slopes of two channels are equal, then finally get:

$$L_1 = \frac{Z_0 \tan(\Delta\phi/2)}{\omega_0}, C_{off2} = \frac{\sin(\Delta\phi)}{\omega_0 Z_0}, L_2 = \frac{1}{\omega_0^2 C_{off3}}, C_{off3} = \frac{2L_1}{Z_0^2} \quad (5)$$

Where the size of the transistor is related to its cut-off capacitance. The 180 °topology circuit is realized by a fifth-order high-pass and a third-order low-pass network. They achieve a phase shift of 110 °and 70 °, respectively. It saves the number of inductors in order to minimize the circuit area [9]. As shown in Fig. 4.

This network provides a degree of phase lag while the one of phase lead is provided by the high-pass network over a wide frequency band. The sizes of the switches were optimized to make the insertion loss of the block equal at both states [10].

Measurement Results

The phase shifter is designed in 0.18*um* 1P6M standard CMOS process. All the phase shift blocks have been cascaded to form the 64-bit phase shifter. Considering the cascade interference between

the phase shift circuits, each circuit performance will be affected by the adjacent phase shift circuit. The phase shift of each block is sensitive to its termination impedance. Thus, the arrangement of blocks in the chain has been selected to minimize their loading effects and the phase error. Finally, in order to improve the overall circuit cascade linearity, small phase shift circuits are placed between the large phase shift circuits, as shown in Fig. 5.The layout area including pads is 2.87×1.2 mm^2.

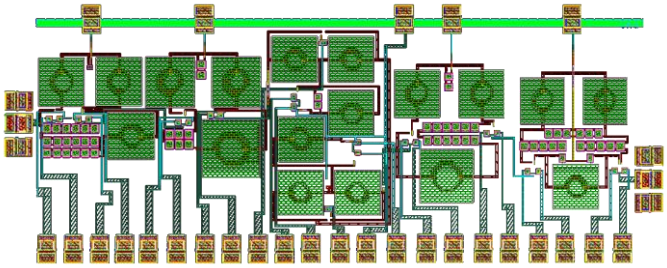

Figure 5. Phase shifter layout

The simulation results including scattering parameters, phase shift and insertion loss of the circuits for the six phase-shifted states are shown in Fig. 6-11.

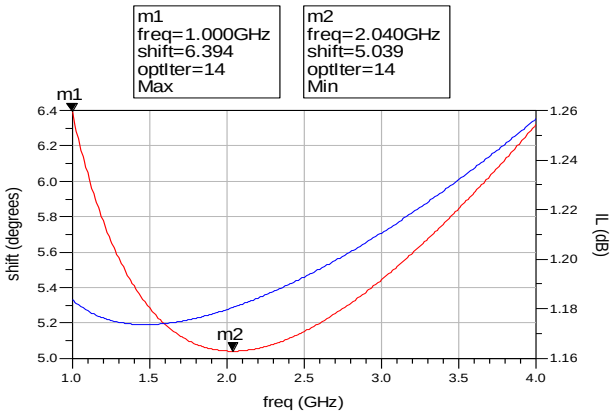

Figure 6. 5.625 °Phase shift simulation

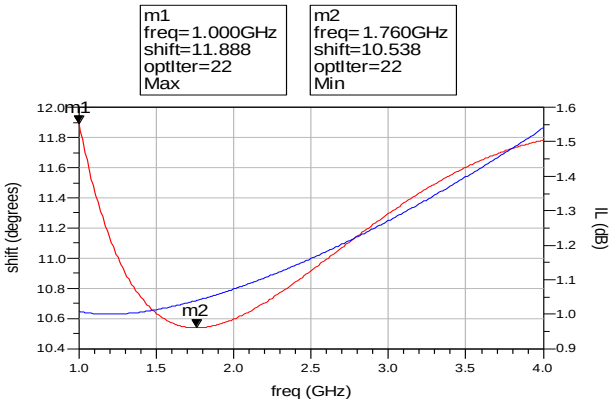

Figure 7. 11.25 °Phase shift simulation

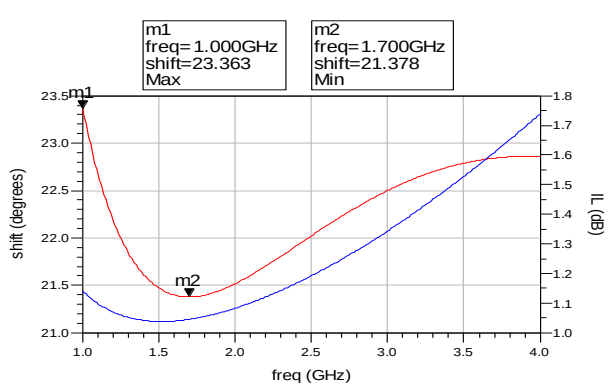

Figure 8. 22.5 °Phase shift simulation

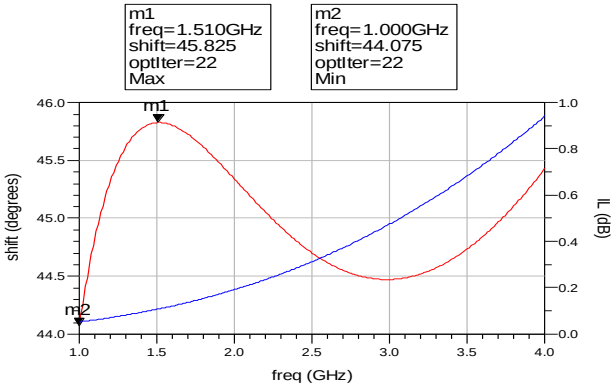

Figure 9. 45 °Phase shift simulation

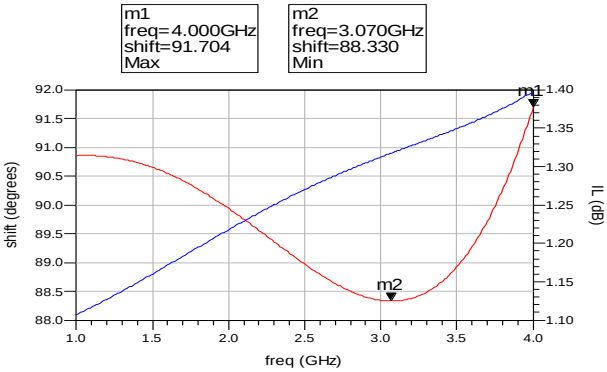

Figure 10. 90 °Phase shift simulation

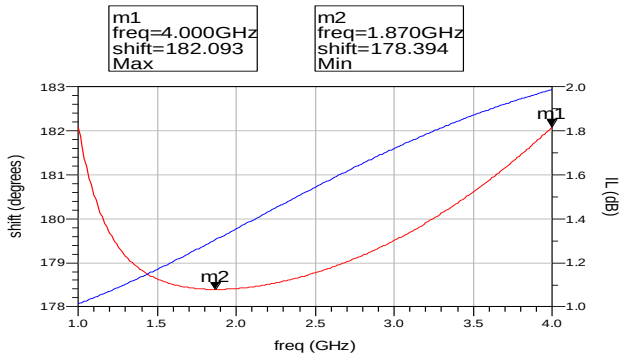

Figure 11. 180 °Phase shift simulation

The measured return loss for L/S frequency band is better than 10 dB at port 1 and port 2. The insertion loss of all the six phase shifts is less than 2 dB. Fig. 12 shows all 64 kinds of phase shifting states. As shown in Fig. 13, it can be seen that the phase shifter has a small RMS phase error which is no more than 2 °at the full operating L/S band.

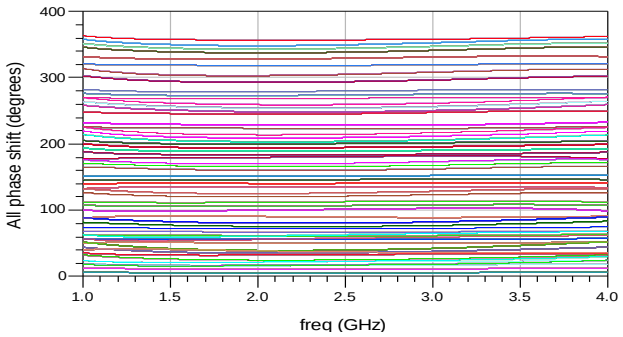

Figure 12. Simulation for all phase shifts

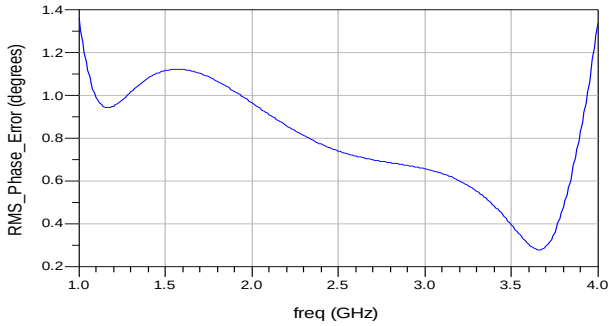

Figure 13. Phase RMS Error

Summary

A 6-bit digital phase shifter which covering L/S band have been designed in a 0.18-um CMOS technology. The 6-bit digital phase shifter design employs the switched-network topology, and can be switched to 64 kinds of phase states in steps of 11.25 ° by controlling the bias voltage. The insertion loss simulation of each phase shift is less than 2dB. And the average RMS phase error is less than 2 °. This work shows the practicality of the phase shifter for the performance requirements of T/R module in phased array radar system.

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