

The Modified digital channelization method

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Abstract: The digital channel receiver must have the ability of processing large number of data , A improved digital channel arithmetic is proposed, This algorithm put digital down conversion before decimation and filtering operation .Moreover the algorithm is realized by using FPGA parallel process. The key design of filter is offered. The result of simulation validate that the algorithm is effective.

1 Introduction

Modern electronic warfare requires access to information faster and more accurate, which requires real-time information on the system detected. However Processing the analog signal requiring amount of equipment, which is difficult to achieve. Digital channelized receiver through the digital processing methods, the use of high-speed processing chip to solve the problem of real-time processing of radar signals and interference signals and improve the whole computing speed. In this paper, We put forward the improved digital channel signal processing algorithms. Which reduces the processing speed based on the original, and solve the problem of real-time processing of the channelized receiver.

2 The principle of the Digital Channel

The basic principle of the digital channels are evolved from the polyphase filter structure. Based on the digital channel from the polyphase filter structure shown in Figure 1. All operations carried out after the extraction, can greatly reduce the signal processing to achieve the difficulty. For complex signals, the entire band for Figure 1

division is divided into the D channel. For the structure shown in Figure 1, Figure 3 shows the equivalent form of the polyphase filter, the frequency shift facto $\omega_k = \frac{2\pi}{D}k$ where $h_p(m) = m(mD + p)$, is the low-pass prototype filter in Figure 2.1 the p-th polyphase branch filter coefficient. $h_p(\frac{m}{2})$ by $h_p(m)$ twice the zero value interpolation.

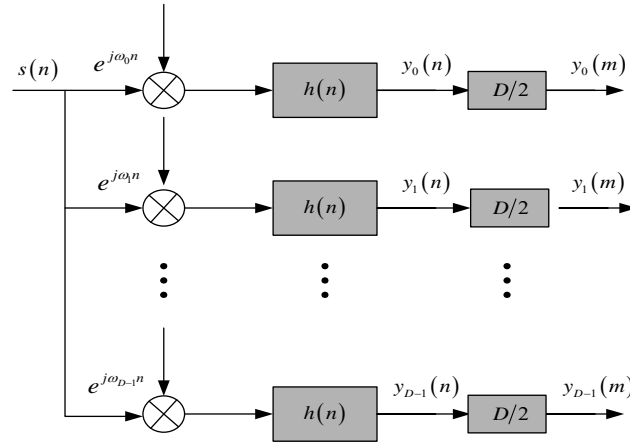


Fig.1 Block diagram of the Digital Channel

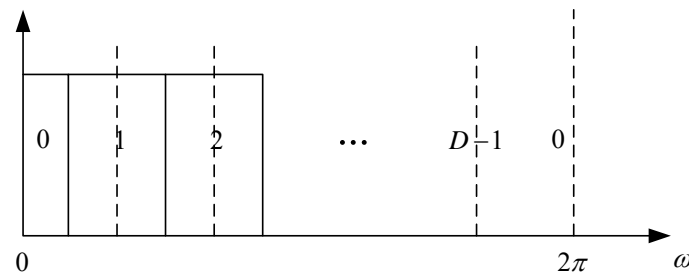


Fig.2 Complex channel division

$$Y_k = \{[s(n)e^{-j\omega_k n}] * h(n)\}_{n=mD'} \\ = \sum_{i=-\infty}^{\infty} S(mD' - i) e^{-j\omega_k(mD' - i)} h(i) \quad 1$$

Make $i=rD+p, p=0, 1, \dots, D-1$, and $D' = \frac{2}{D}$ generation (1)

Define:

$$y_k(m) = \sum_{p=0}^{D-1} \sum_{r=-\infty}^{\infty} S(mD' - 2rd' - p) e^{-j\omega_k(mD' - 2rd' - p)} h(2rd' + p) \\ y_k(m) = \sum_{p=0}^{D-1} \sum_{r=-\infty}^{\infty} s_p(m - 2i) h_p(i) e^{-j\omega_k(mD' - 2iD' - p)} \\ = \sum_{p=0}^{D-1} [S_p(m) e^{-j\omega_k mD'}] * h_p\left(\frac{m}{2}\right) e^{j\omega_k p} \\ = \sum_{p=0}^{D-1} [S_p(m) e^{-j\omega_k mD'}] * h_p\left(\frac{m}{2}\right) e^{j\omega_k p} \quad (2) \\ \text{To get } \omega_k = \frac{2\pi}{D} k \text{ into the formula 2} \\ y_k(m) = \sum_{p=0}^{D-1} [S_p(m) e^{-j\omega_k mD'}] * h_p \\ = \sum_{p=0}^{D-1} [S_p(m) e^{-j\omega_k mD'}] * h_p \\ y_k(m) = \sum_{p=0}^{D-1} [S_p(m) e^{-j\omega_k mD'}] \\ = \sum_{p=0}^{D-1} [S_p(m) * h_p\left(\frac{m}{2}\right) e^{j\frac{2\pi}{D} p}]$$

$$=[\text{IDFT}(S_p(m) * h_p(\frac{m}{2}))](-1)^{mk}$$

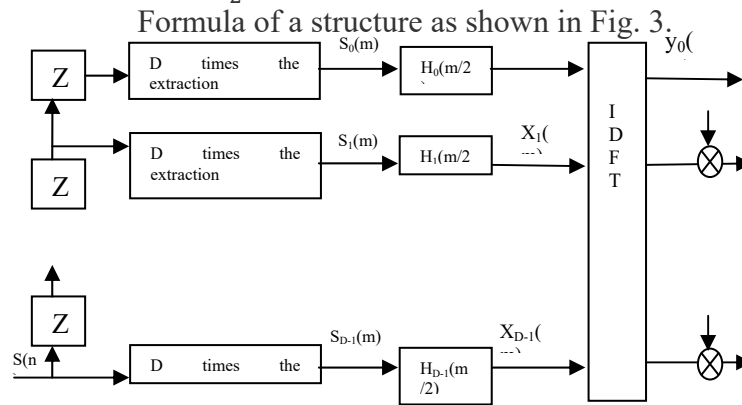


Fig.3 Channel of the algorithm implementation

A simple understanding of this method is :first, according to the number of chanel required for a certain division of the frequency band, for the real signal sampling rate of FS system, the maximum effective bandwidth of $fs/2$.if the effective bandwidth of $fs/2$ is divided into N channels, the bandwidth of each channel is $fs/N/2$.Center frequency is $n*fs/N/2$, which $n=0...N-1$.In the process to obtain the M channel information, the center frequency of the channel from $m*fs/N/2$ moved to 0 frequency. namely the A/D sampling data obtained by multiple factors that, then the required data channel by using a low pass filter to filter, and a certain amount of data extraction. Way to bring the different is different channels differ in frequency shifting multiplied in mutiple factors. And the complex number is exactly the factor of $2N$ point FFT operation. If you want to split the 64 channel , you need to be 128 times the low pass filter extraction ,and 128 point FFT.

For a signal channel , assumes that the data receiving unit receiving bits 8bit,rate 1000MHz data stream from the output of A/D, then send it into the extraction rate for 128 polyphase filter to process .Filter design according to between the number of channels and adjacent isolation needs to design, generally low pass filter, with MATLAB software to determine the filter coefficients and filter coefficient divided into group of 128,as shown in Figure4.

The input data $x(n)$ 128 times speed reducing shunt, income of 128 low-speed data streams, respectively ,into the 128 filter group,128 filter bank output of 128 points FFT exchange, the resulting outputs $Y(0)$ to $Y(63)$ corresponds to the value is the result of the 64 channel output channel.

3 Improvements of the channelized approach

3.1 The channelized algorithm design.

And similar to the principle of the previous section, we used in the concrete realization of an improved way: first 1GHz data stream of the A/D acquisition proceeds, IF 750MHz real signal of the digital down-conversion processing, move to the 750MHz IF frequency 0 and 2 times decimation filter processing to obtain 500MHz baseband I and Q complex signal data stream,and then the signal64 times deceleration shunt treatment, from the 64-way low-speed data stream into 64 polyphase filter group; The output of the 64 filter banks is carried out 64 points of the FFToperation, the resulting output $Y(0)$ to $Y(63)$ is 64 channel output.Which increases the down-conversion processing chain, but it reduces the back-end processing speed requirements and FFT operation points.Figure 5/6 shows the block diagram of the quadrature down-conversion and 64 channels.

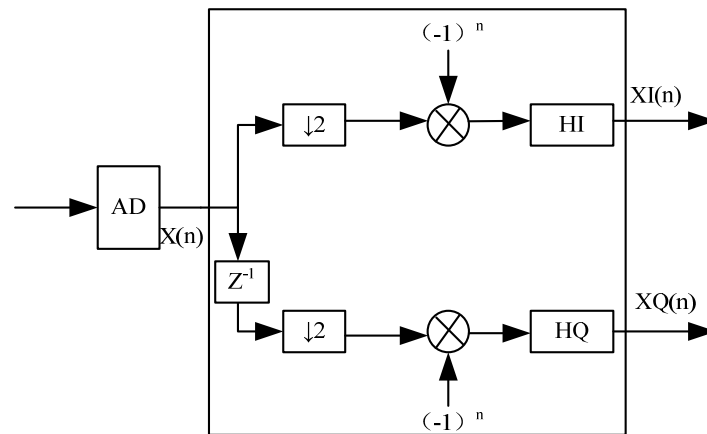


Figure 4 Digital Quadrature Frequency Conversion

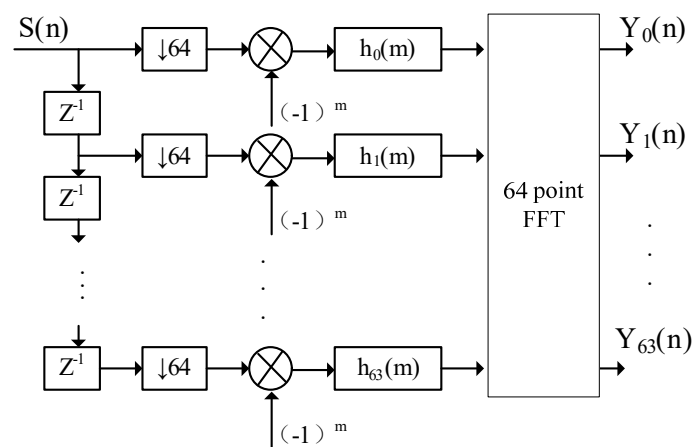


Figure 5 64 Channel Chart

3.2 Times extracted anti-aliasing filter design

In the filter design, the MATLAB FDATool tools to the design parameters are as follows: filter type: LOWPASS; $F_s = 1000\text{MHz}$; $F_{\text{pass}} = 200\text{MHz}$; $F_{\text{stop}} = 250\text{MHz}$;

band ripple: 0.3 dB; band rejection: 60dB. As shown in Figure 7, the design proceeds of the filter order of 48 bands.

3.3 Polyphase filter design

Using MATLAB FDATool tools to design, select the following parameters: filter type: LOWPASS; $F_s = 500\text{MHz}$; $F_{\text{pass}} = 3.9\text{MHz}$; $F_{\text{stop}} = 7.7\text{MHz}$; band Ripple: 0.5dB; band rejection: 50dB. As shown in Figure 8, the design proceeds of the filter order of 256 levels. The filter coefficients $h(0:255)$ into 64 groups, means of distribution as: Part i of the filter coefficients k -th coefficient is:

$$h_i(k) = h(64*k + i).$$

3.4 IP 64 points FFT arithmetic design

There are many 64-point FFT implementation in an FPGA, you can build, according to the algorithm can also be provided by the FPGA development software IPCORE. In order to reduce design content, choose the latter to achieve. FPGA development software free IP CORE general single-input, water treatment single IPCORE can handle the data rate of the processing clock of the module, a decision for the VIRTEX6 series of devices to handle the clock is generally up to about 300MHz. If the data rate requirements 1GHz, 4 IPCORE parallel processing can be used to achieve. The concrete realization of the structure shown in Fig.7

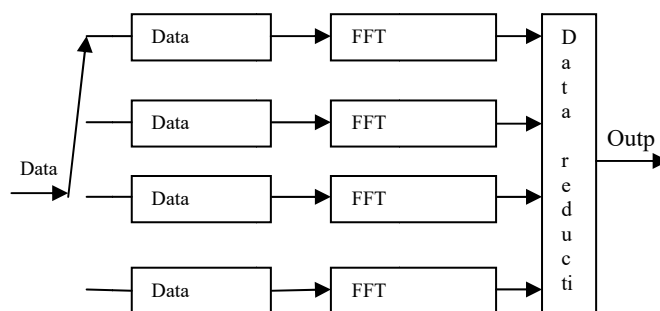


Fig.6 64 FFT

In Figure 7, each data cache unit is divided into A, B, the two areas. Start first data

rate of 1GHz, into a Zone A data cache to store until the full 128 data to the data cache 2 Zone A, and at the same time start FFT IPCORE1 to 250MHz rate of flowing water area A, take the data model from the calculation; so turn down, when the data cache is full data of the 4 area A, an area B data Bian xiang data cache store, area B is full, the data stored in the data cache in area B 2, the FFT IPCORE1 just completed on the data cache 1 zone A data extraction, began to take data from area B to calculate, and so on. After a certain amount of computing time from the output of the FFT IPCORE the results of the FFT operation

3.5 The channelized results of simulation

Input signal frequency: 760MHz and 800MHz signal (analog signal) Spectrum showing the output of each channel, the vertical axis represents the spectrum amplitude (dB).

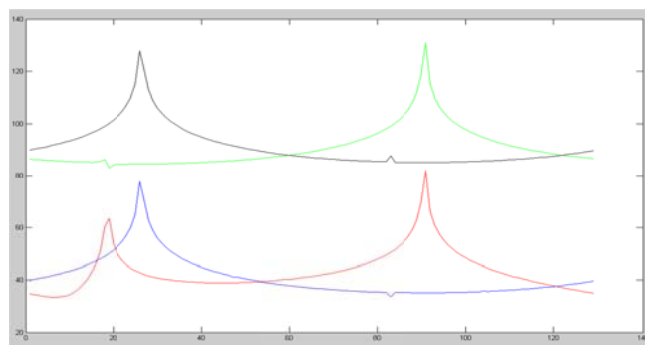


Fig.7 Display 5-8 channel spectrum

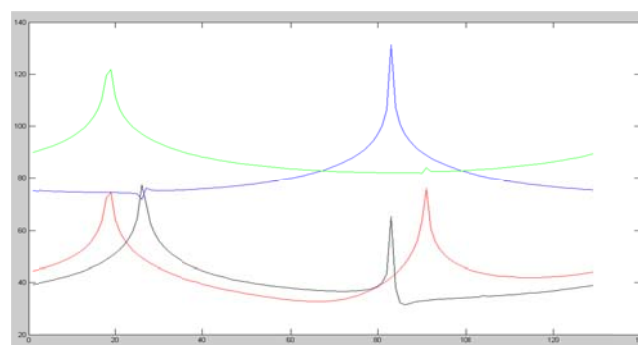


Fig.8 Display 5-8 channel spectrum

750 Mhz IF, 64-channel processing system should be located on the second channel in the 760MHz, 800MHz should be located in the channel. It can be seen from Figure 8, 9, simulation results are consistent with the theoretical analysis, the transition zone in the process of division of the channel filter, the signal attenuation between the adjacent channel is not, the interval between the channel signal rejection is 50dB, and design consistent with in hibition of in-band filter 50dB. In the back-end of the channel selection process can be simple to judge between the adjacent channel signal strength to determine the attribution of the signal channel.

4 conclusion

This paper analyzes the basic principle of the channel, the channel of a flexible approach,

given the design of key modules of the algorithm. Simulation results validate the effectiveness of the algorithm. This article only gives the realization of a common digital channel, but further research is needed for signal detection of the same channel and broadband cross-channel signal detection

References

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