# Bottom-up copper plating to form stacked interconnection of HDI printed circuit board for optical module application

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**Abstract :** Plating factors of graphic design of copper patterns and plasma pretreatment of dry film were investigated to find their effects on bottom-up plating quality of copper pillars. The thickness of copper pillars is examined using scanning electron microscope. John's Macintosh Product software is used to analyze the thickness distribution of the copper pillars on the surface of the base board. Graphic design of less copper pillars in the surface, dry film with the thickness of 100  $\mu$ m and two-time plasma pretreatment of dry film could result in good plating pillars for stacked interconnection of printed circuit board (PCB). High density interconnection (HDI) PCB can lead to high-speed signal transmission during optical module application.

### 1. Introduction

Printed circuit board (PCB) needs to form stacked interconnection in order to meet the requirement of high-speed signal transmission during optical module application. Copper plating with good reliability and electrical performance [1-6] is used to form stacked structure between PCB layers for high density interconnection [7,8].

The quality of copper deposits is generally limited during copper electrodeposition due to the influence of plating parameters, formula, pretreatment and pattern design. Organic additives are added to plating solution to generate good synergetic effect of copper deposition. Recent researches reveal that bottom-up copper plating is one of good methods to fill microvias for interconnection [8-11]. However, pretreatment and pattern design could also play an important role in the quality of copper plating since current distribution could be uneven in the surface of cathode.

The purpose of this paper was to investigate the quality of bottom-up copper plating to obtain good interconnection. The thickness distribution of copper pillars is measured to analyze the effects of graphic design of copper patterns and plasma pretreatment of dry film on final copper deposits.

### 2. Experimental

As shown in Fig. 1, bottom-up filling for z-interconnection was realized after copper electrodeposition inside the microvias of dry film in the way of semi-additive process.

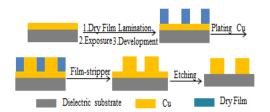
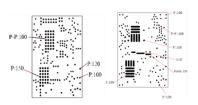


Fig. 1 Bottom-up plating copper pillars by semi-additive process





(a) design I (b) design II Fig.2 Two different kinds of graphic design for copper electrodeposition

The tested base boards with 1- $\mu$ m-thick sputtered copper layer were approximately 505 mm×405 mm in area for copper electrodeposition. Copper electrodeposition was performed in a plating line with air agitation at the current density of 12.1 mA/cm² for 300 min. 75 $\mu$ m (+15/-10 $\mu$ m)-thick copper pillars were deposited to evaluate the thickness quality of copper deposits on the boards. Every board was measured 9 points of copper pillars with 100 $\mu$ m in diameter.

Plating factors of graphic design of copper patterns and plasma pretreatment of dry film were investigated to find their effects on bottom-up plating quality of copper pillars. Two graphic structures, defined as I and II, were designed to carry out the plating tests, as illustrated in Fig. 2. Difference between two kinds of design was the copper pillar distribution. Dry films with 100µm and 75µm were used for the plating formation of interconnecting microvias, respectively. Plasma pretreatment of dry film is also needed before copper electrodeposition.

Scanning electron microscope was performed to observe the thickness and the microstructure of copper pillars and the surface of dry film. John's Macintosh Product software is used to analyze the thickness distribution of the copper pillars on the surface of the tested base boards.

### 3. Results and Discussion

### 3.1. Effect of graphic designs on copper deposition

Bottom-up copper plating quality from  $100\mu m$  dry film in two different graphic designs was evaluated after one-time plasma pretreatment of dry film. The average (AVE) thickness of copper pillars with the diameter of  $100\mu m$  was observed from 4 tested boards (1#, 2#, 3# and 4#), as displayed in Fig.3.

The target value of thickness of copper pillars was 75 $\mu$ m. The thickness of copper pillars from the tested boards with two graphic designs is larger than 75  $\mu$ m. All the thickness of copper pillars meets the target value of thickness of 75 $\mu$ m (+15/-10 $\mu$ m). However, the case for Design II exhibited good uniformity on the plating thickness of copper deposits. The tested boards with Design II had less copper pillar, thereby leading to uniform distribution of current to form the even copper deposits inside microvias of dry film.

# 3.2. Effect of dry film on copper deposition

Effect of dry film on copper deposition with different thickness was investigated in the condition of one-time plasma pretreatment of dry film from graphic design II. The target value of thickness of copper pillars was also 75μm. Copper pillars had good agreement with uniform AVE thickness when using 100-μm-thick dry film for the formation of interconnecting microvias, as shown in Fig. 4. In addition, nip phenomenon could occur since the thickness of copper deposits was larger than that of 75-μm-thick dry film. Thus, 100-μm-thick dry film could lead to good quality of copper deposition.



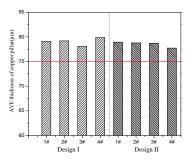


Fig.3 AVE thickness of copper pillars from different graphic designs

Fig.4 AVE thickness of copper pillars by the different thickness of dry film

## 3.3. Effect of plasma on copper deposition

Plasma process for plating pretreatment plays an important role in electrochemical deposition of copper pillar. The times of plasma pretreatment were evaluated to find the influence on copper deposition. As displayed in Fig. 5, the AVE thickness of copper pillars was larger than 80µm after one-time plasma inside the 100µm -thick dry film. However, the case for two-time plasma resulted in the thickness of lower than 80µm for copper deposition. The surface morphology of dry film after different times of plasma pretreatment was shown in Fig. 6. The process of exposure and development could lead to residue on the surface of dry film. It is difficult to completely clean the residue on the bottom of dry film after only one-time plasma pretreatment. Copper deposits could be easy to form the smaller surface inside microvias of dry film, thereby generating rapid copper deposition. However, when the residue of dry film was well cleaned after two-time plasma pretreatment, copper deposition was inhibited to form completely filling inside microvias of dry film.

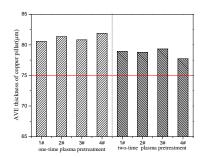


Fig. 5 The thickness of copper pillars by the different times of plasma

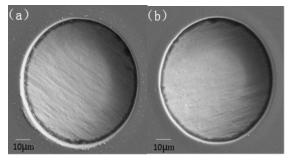


Fig. 6 SEM images after different times of plasma: (a) one time (b) two times

# 3.4. Influence of three factors on electrochemical deposition of copper pillar

According to the above three experiments, the fourth group experiment were carried out in the best conditions of graphic design II, 100- $\mu$ m-thick dry film and two-time plasma pretreatment. The AVE thickness of copper pillars was about  $78\mu$ m.

John's Macintosh Product software (JMP) was used to calculate the Process Capability Index (CPK) of the thickness data. From the analysis result of these data in Fig. 7, CPK was 1.52 which conformed to the requirements of the production line process. In above best condition of copper deposition, bottom-up copper pillars exhibited good agreement with uniform thickness. Fig. 8a displayed a copper pillar with the thickness of  $78.5~\mu m$ . Cross section of bottom-up copper pillars in Fig. 8b indicated that high density interconnection was formed from copper electrodeposition in the best condition.



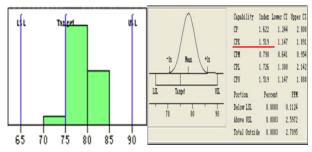


Fig. 7 CPK of the fourth experiment by JMP

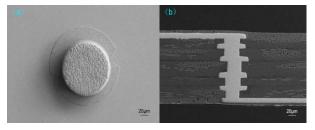


Fig. 8 The SEM of bottom-up copper pillars.
(a) Top views of bottom-up copper pillars;
(b) Cross section micrograph of bottom-up copper pillars and patterns for inter-connects of IC substrate.

### 4. Conclusions

Uniform plating bottom-up copper pillars was generated when the condition of copper plaited was chosen as graphic design II, 100-µm-thick dry film and two-time plasma pretreatment. High density interconnection was carried out to meet the requirement of high-speed signal transmission for optical module application.

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