ATLANTIS PRESS
Advances in Computer Science Research, volume 71
4th International Conference on Machinery, Materials and Information Technology Applications (ICMMITA 2016)

Control System of Intelligent Vehicle by Panoramic Vision

Yubin Zhou
Shanghai University of Engineering Science, Shanghai, 201620, China
email: choybeen@yahoo.com

Keywords: Intelligent Vehicle, Vehicle control, Panoramic vision. Driverless Vehicle

Abstract. The success of driverless mainly depends on the intelligent visual system which can control car on the road as we human do. A high efficient controlling system based on panoramic vision for intelligent vehicles, supporting 8 cameras at most, is presented in this paper. The visual module is composed of a FPGA and two DSP to carry on the massive high speed parallel processing for panoramic image construction. The system realizes the intelligent vehicle control with real time panoramic image reconstruction and road lane detection. Central controlling module connects all the sub-system by CAN bus, while the visual module is one of the sub-system. During the driving on the road, the lane lines are detected from the panoramic image and tracked on each following frame. Parameters of the deviations are sent to the main control node as soon as the car goes off the course, then the control signal is decoded and sent to the sub-system for further operation such as corresponding steering device or ABS. Bidirectional gated channel on the sub-controlling-system receives real-time signals from sensors of the mechanical positions while the actuator controlling the car to verify the control precision. The correction mechanism responds rapidly to the changing of the lane to keep the car running on the right lane. And the embedded system μC/OS on the central module manages the balance of multitasks for the high speed automatic control of the intelligent vehicle.

1 Introduction

The intelligent electronical control system of the driverless vehicle is composed of the road recognition and high speed control communication circuit. The road recognition device identifies the lanes from the complex road conditions, according to the requirements of the use of the steering rudder angle, speed, acceleration and other signals, to control the car to achieve automatic driving. Vision based driverless vehicle has a good application prospect in the future since it can improve the safety of automobile and more economic.

In the past few years as the limited hardware computing resource, monocular vision is a better choice for driverless vehicle. But the information of monocular is also very limited for complex algorithms. Multi vision, on the other hand, can “look” around the car at any time during driving and has been gradually replace the monocular system. This paper introduces an intelligent navigation electronic system for driverless vehicle with 8 high-definition cameras at most. The panoramic image from those 8 cameras can observe around the vehicle 360 degrees seamlessly. The control system includes a central module and many other peripheral subsystems, such as air conditioner, multimedia and visual modules. All those modules are linked with CAN bus for communication. The vision module is composed of two pieces of C6416 DSP chip and a high performance of Virtex-4 FPGA that can meet the real-time requirements of complex processing[1,2]. After reconstruction of cylindrical panoramic image, lanes are detected from the panoramic image and position parameters are sent to the main control module for further controlling to keep the car on the right lane for safety. Vision module can do many other processing, including detection of pedestrians, cars, and recognition traffic lights, signs and etc.

The rest of this paper is organized as follows. Section 2 introduces the whole control system includes the vision module; Section 3 describes panoramic image construction methods and results; and Section 4 gives the lane detection and navigation control. Section 5 concludes with future research directions.

2 System scheme

Vehicle control system includes a central module and many other sub-systems for various functions, such as power support, air conditioner, security and other subsystems. The whole system connects together by CAN protocol for communication as shown in Fig.1. All subsystems are independent to each other to control their own devices. The panoramic vision module as one of the independent subsystems consists of a high-speed FPGA and two DSPs. After agreement from the main node on the requests from vision node, then it links to the control device directly on CAN bus and transmits the detection parameters of road lane for controls without the main module's interfere.

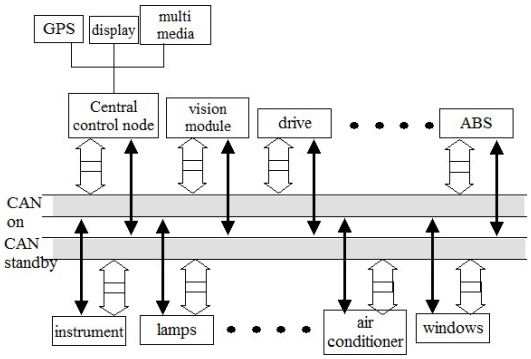

Fig.1 Star network topology of control system

2.1 Star network of control system. The control system scheme is star network topology, Freescale MCU, XEP100 dual core chip at 24M, is on central module with peripherals as power supply, IO interface, multimedia and others. For convenience of debugging, it links to keyboard, display by BDM and COM I/O. Sub-system are node circuit boards for variety of signal and sensor interface, including A/D, D/A, PWM output, CAN. A built-in logic coprocessor XGATE in MCU operates with the core processor that can respond to external interrupt signal without interfere of the core processor which greatly improves the system response speed[3,4].

The central module as the main control node works in two states, the external command control and autonomous control. In external command state, it accepts signals from keyboard or touch screen for manual control, and sends those commands to the corresponding subsystems. In the automatic mode, control parameters and commands received from the intelligent visual module by the CAN are decoded and redirected to the corresponding node for further control. In both states, device parameters and states are sent from other peripheral nodes to the central module to watch alarms or instruction requests.

The subsystem module operates as functional circuit node responsible for the analysis of all the received commands, and executes those instructions at the same time. During the control operation, the state data of implemented control from sensors were compared with expected ones to verify the execution results. The subsystem module corrects the control actions until it reaches the accuracy. In addition, the node is responsible to monitor the state or control mechanic and send the work state to the central node to confirm their states in order. When there is state not in normal, it informs alarm signals to the central node and requests for further processing instructions. The system uses redundant CAN bus for serial connection in case of the unexpected mistakes. Two CAN buses are enabled, however, only one is in real work state while the other is standby for backup. All the nodes receive the heartbeat signals for implementation of CAN communication. When errors occur on the active CAN bus, such as no heartbeat signals more than 3 timeout, all the nodes in the system switches to the standby CAN immediately according to the commands from central nodes[4,5]. When the system starts, messages from all subsystem make sure their states in order after self-check. Then the center node allocates registers for each sub-node and displays their states on the screen or by lamp. After all nodes initializing finished, central node waits the new requests and heartbeats from all sub-nodes on CAN bus.

2.2 Vision subsystem The panoramic vision system consists of a high-speed FPGA and two DSP, as show in Fig2. The FPGA is XC4VFX60-FF1152 from Virtex-4 series, the inner PowerPC support most embedded OS like VxWorks, Linux, work as the SoC for the vision system to load the starting

software, task assignment and operation logic controlling. The DSP C6416 has eight parallel processing units, working in 1GHz responsible for the needed processing like the floating-point and fixed-point algorithm.

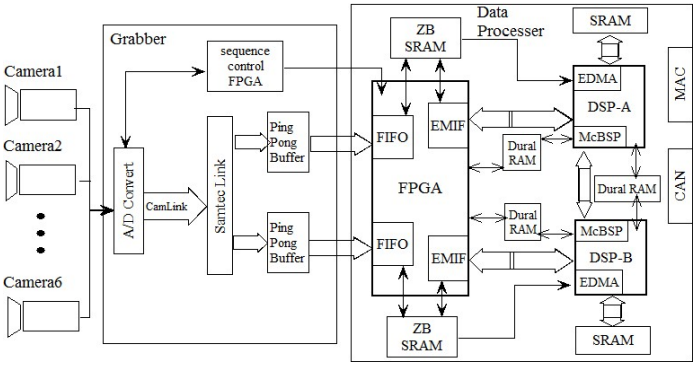

Fig.2 Vision system

The FPGA focuses on image data conversion, filtering, and other preprocessing tasks. And then transmits the preprocessed data into its internal FIFO. The DSP starts the EDMA to transfer data to the DSP on-chip Cache as soon as the data transmit FIFO data reaches the threshold amount without interrupting the CPU core. This straight-through data transfer structures can be easily adapted to multi-camera acquisition and processing system.

When system powers on, FPGA loads the operating system first, then inform the two DSP to load their software, and begin to wait for the frame ready signal from image capture module. Once the ready signal is received, the data transfer model in FPGA start to move data to ZBT-RAM and inform the processing model to work. This high-performance architecture of DSP+FPGA for parallel data processing can be easily to complete the complex application like cylindrical panoramic vision needed for intelligent vehicle in real-time processing.

3 Panoramic image generation

Six cameras around the vehicle in 6 directions for panoramic vision capture the surrounding images and the vision system project to generate cylindrical panorama. However, because the distributed camera mounted on the vehicle is not fully meeting the same point of view, even the viewpoint among the three front or rear cameras are different with a certain distance. The cylindrical panoramic project matrix can be corrected by the parameters from image registration between two neighboring images[5,6].

3.1 Cylindrical transformation. The general panorama generation process mainly including image acquisition, image mosaic, image fusion of overlapped area. All images can be warped perspective to the cylindrical surface. Ideally, only the unknown panning angles need to be recovered by the overlapped area of adjacent images to build a cylindrical panorama from a horizontal panning sequence. But in practice, small vertical translations are needed to compensate for vertical jitter and optical twist because the camera's viewpoints are not from one point, as camera A and camera B shown in Fig3. Therefore, both the horizontal translation dx and the vertical translation dy should be estimated for each input image from the corresponding features. The displacement in two directions and rotation can be derived from the set of matching-feature pairs been generated above in 2.1. Image rotation transformation is applied to each inputting image in order to eliminate the rotational components as well as the displacement by H_a before cylindrical projection. Therefore, after eliminating the rotation and height deviation, the camera's motion can be seem as 2D translation. This will make the latter mosaics image easier.

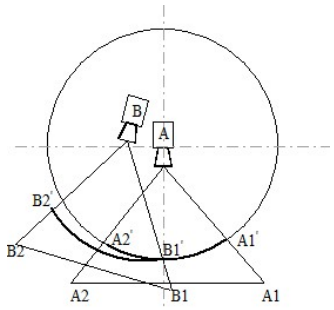

Fig.3 projection errors

The ideal cylindrical projection of image transformation is Eq.1 below:

$$P_d = P_0 H_d \tag{1}$$

In Eq.1, P_0 is the original image, P_d is the cylindrical surface image, H_d is the conversion matrix. The ideal projection need to be rectified by H_a. The new conversion matrix is Eq.2:

$$P_d^{'} = P_0 H_d^{'} = P_0 H_d H_a^{-1} \tag{2}$$

$H_d^{'}$ is the new matrix rectified by H_a. After the image registration, all the rectified transformation matrix $H_d^{'}$ are stored in the external memory, and read to inner memory when the system startup each time. During the image mosaic for panoramic, the conversion task is strong parallelization process in FPGA in pipeline for floating point of all pixel values.

3.2 Panoramic image stitching. There is a certain overlap area between two adjacent images from camera around vehicle. The common features such as Harris or SIFT algorithm are stable, robust for most scene. In particular, SIFT feature, which is good at invariance of uniform scaling, orientation, partially invariant to affine distortion and illumination changes. It is commonly used in image matching, and can be used in image stitching for fully automated panorama reconstruction from non-panoramic images[7]. The SIFT algorithm is complicated and computation time is long. The original SIFT algorithm should be significantly optimized for high efficient implementation on FPGA to meet the real-time video processing. Some steps are executed by pipeline of different algorithm processing model in FPGA. Each processing model, such as Gaussian filter, can process 8 lines in FPGA parallel.

Reduce the total dimension of the feature descriptor of the original SIFT which simplify the image matching operation significantly. Limit the SIFT processing only in the overlapped area can reduces the computation time obviously too, shown in Fig4. All feature date set are saved in the FIFO and transmitted to DSP. In the DSP, the four most matching pairs of feature are selected by RANSAC algorithm for projection matrix H_a.

(a) Features overlapping (b) Panoramic result

Fig.4 Panoramic image construction

4 Lane detection and tracking

There are two scenarios about autonomous driving for intelligent vehicles: on the road and off the road. Only autonomous driving on city road with clear lane mark is discussed in this paper.

4.1 Hough line detection The Hough transform based lane detection is the common way that can detect the lane from the images of the front road[8-10]. Both straight line and curves can be detected along with this Hough Transform. Although Hough transform has strong adaptability, but the algorithm is time-consuming for real-time processing and lead to many errors when the lane is not clear or objects in the road, as the result Fig.5b shown. The canny edge detection with a threshold value is applied to pre-process the inputting frames. The probabilistic Hough transformation is applied on image subarea to extract the main direction of traffic lanes, choose the most possible statistical lines to segment the lane areas for driving, as shown in Fig.5c.

(a) original image (b) first result (c) last result

Fig.5 Hough detection results of lane

The Hough detection of lane detection techniques are edge based, subsequent to the edge detection step of the whole process. Preprocessing including image filtering, threshold, edge detection and etc., can be processed parallel by FPGA before image stitching. Then the DSP perform the Hough transform for lane detection[10,11]. In order to make it fast enough to processing for real time applications, the procedure is optimized additionally. 1) The area constraints. Since the driveway with a certain range of angles in the camera screen, limited the polar angle of left and right lane and the radius, can reduce the computation. 2) Computation in quantify. In a certain range of accuracy, quantify the parameter ρ and θ within the range values to many rectangular regions for accumulation in the parameter spaces for detection, but not the floating-point value. Finding the rectangular regions with maximum accumulated value determines the possible lane. 3) Lane tracking. Due to the continuity of the vehicle driving, once the lane found, predict the lane position in the subsequent frames[12,13].

4.2 Multi control tasks management It is vital for the vehicle control system to work in real-time operation, so the μC/OS system used for those complex multi-task management to improve performance of the whole control system[14]. The μC/OS is portable, curable, especially on multi-task processing for real-time operating system(RTOS). It can supports as much as up to 64 tasks as the same time, and the communication mechanism is variety enough for different procedure, such as the semaphore, mailbox and message queue among multi processers. The signals have different priority on the CAN bus, signals for control is higher while the information content such as display or some alarms is lower. And those priorities are homologous to the priority of processing tasks. All the requests of control command are always with high priority to ensure that the system can deal with the emergencies in time for safe. Tasks are defined with priority in for scheduling in the queue, which allows the highest priority task ready to occupy processor resources for running. But the emergencies are special tasks could never wait for response. Those tasks would be triggered by interrupts and processed by coprocessor XGATE in MCU.

5 Conclusions

With the progress of electronical technologies and improved vehicle safety requirements, active security systems based on the visual system became increasingly more and more popular. As one of the sub-node in the control system of driverless vehicle, the vision system works dependently with high performance processors DSP and FPGA for the very critical requirement of automobile. Any electronical troubles would not affect the central control system to cause any driving problems. The high speed CMOS with FPGA and DSP reduces the classical bottleneck between sensor and processing. The FPGA component ensures a high parallel processing and DSP for fix-point low-level

processing. The intelligence of vision system assists vehicle to keep the driving line on the road lane, and it also help the obstacle avoidance and any traffic accidents of human knocking. In the future, the autonomous vehicle on the road drives on the road like human being could do, traffic signs recognition is another Challenge needing more sophisticated algorithms, such as the depth neural network. The hardware with higher performance for vision system becomes the later application research for safer automatic driving.

References

[1] G Zhou. Design of HD-SDI High-resolution Image Processing System Based on FPGA and DSP, Microcontrollers & Embedded Systems, Vol.23,No.8, 2014. pp117-122

[2] Xianbo Zhou, Longling Feng, A study on image acquisition technology based on DSP and FPGA, Optical Technique, Vol.32(Suppl), 2006. pp141-143

[3] V. Miñambres-Marcos, I. Roasto, P. Szczepankowski, Code development of a DSP-FPGA based control platform for power electronics applications, IEEE International Conference on Industrial Technology (ICIT), 2015

[4] R. C. Chaubey. Computerized Image Analysis Software for the Comet Assay, Molecular Toxicology Protocols, ISSN 1064-3745,2008, 291

[5] Sandesh S Saokar, R M Banakar, Saroja V Siddamal. High speed signed multiplier for Digital Signal Processing applications. IEEE International Conference on Signal Process. 2012:1-6

[6] Xing-yao Chen, Zhen-hua Wang, Jin-wen Tian and etc. Design of a ZBT SRAM controller for high speed remote sensing image compression system. Microelectronics & Computer. 2005, Vol.22(3).pp46-49

[7] Cheng Zhang, Chunping Hou, Xiaoyan Wang, and etc. A setup for panoramic stereo imaging. Multimedia Tools and Applications. Vol. 75, No12 (2016), p. 6945-6962

[8] Li Lv, Tanghuai1 Fan, Xin Wang and etc. An algorithm for generating cylindrical panoramic image based on double projecting in images with single view. Journal of Nanchang Institute of Technology. Vol.32, No.6 (2013), p12~16

[9] Yi Zou, Yong Chen. Hua You. A Fast SIFT Image Mosaic Algorithm Based on Wavelet Transformation. Journal of Chongqing Normal University.Vol.31(3),2014. p12~16

[10] Gurjyot Kaur, Amit Chhabra. Curved Lane Detection using Improved Hough Transform and CLAHE in a Multi-Channel ROI. International Journal of Computer Applications. Vol.122,No12, 2015, pp32-35

[11] Vincent Voisin, Manuel Avila, Bruno Emile and etc. Performance Evaluation of Modified Hough Transform for Road Lane Colorization. International Journal of Advanced Research in Computer Science and Software Engineering. Vol5(7), 2015, pp150-159

[12] Amit Bhati, R.K. Somani. Partition based Hough Transformation for Real Time Road Lane Detection. International Journal of Electronics and Computer Science Engineering (IJECSE),Vol.2, No.4,2012,2014.pp1117-1122

[13] J.C. McCall, M.M. Trivedi, Video-based lane estimation and tracking for driver assistance: survey, system, and evaluation, IEEE Transactions on Intelligent Transportation Systems, Vol.7, Issue-1,2006,pp20-37

[14] Minde Zhao, Zhaohui Wu,etc.SmartOSEK: A Real-Time Operating System for Automotive Electronics[C]. Lecture Notes in Computer Science. Vol.3605. 2005,p437～442.