High-efficiency Rectifier for Passive RF Energy Harvesting Devices

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ABSTRACT: In this paper, a highly efficient differential rectifier for passive radio frequency (RF) energy harvesting device is designed. The circuit uses the differential-drive CMOS to reduce the RF energy loss caused by the MOS threshold voltage during rectification and improve the rectification efficiency of the circuit. The circuit was fabricated with a 0.35μm CMOS process and the overall RF-DC power conversion efficiency for a DC output power of 160μW (2.5V and 64μA) is about 50%. When high voltage is needed for stimulator output, the maximum efficiency for a 4V DC voltage reaches 66.5% at -3dBm. The proposed rectifier allows the output voltage higher than 6V. It is suitable for such applications that require high RF input power such as implantable medical devices (IMDs) and passive industrial sensor.

1. INTRODUCTION

There is various RF power devices have been developed for different applications, such as implantable stimulators, industrial sensor, etc. For particular application which requires high level power consumption (higher than 1mW), the battery may lead many limitations. These problem can be overcome by using RF energy harvesting which is the process of receiving energy from the transmitter. Many researches transfer power by inductive coupling coils to achieve high power transmission efficiency [1]. It lead device's size considerably large. The UHF band (860-960MHz) is used to minimize device size and preform higher efficiency. The available power can be theoretically calculated by the Friis transmission equation

$$P_r = G_r \times P_{EIRP} \times \left(\frac{\lambda}{4\pi R} \right)^2 \tag{1}$$

Where λ the wavelength of the EM wave, R is the distance between transmitter and receiver, P_{EIRP} is the effective isotropic radiation power of transmitter and G_r is the receiver antenna gain. P_{EIRP} is determined by regional regulations and G_r is determined by the antenna design (2dBi for $\lambda/2$ dipole antenna). For our cases, the available power received by antenna is assuming less than 5dBm and antenna gain is 1.64dBi. The PCE is used to represent the rectifier's power efficiency and the detail will discuss in section III

In this work we design a high efficiency differential drive threshold voltage (V_{th}) cancellation rectifier circuit with regular voltage output and the circuit is compared with a conventional rectifier based on Dickson charge pump. Both of these circuits have been fabricated in 0.35μm CMOS process.

This paper is organized as follows. In Section II, we discuss the basic operation of conventional rectifier and how power loss in high voltage stimulator. The proposed rectifier circuit description is given in Section III. In Section IV we summarize our circuit performance and compare it to the control group result. Finally, Section V summarizes our overall conclusions.

2. CONVENTIONAL RECTIFIER CIRCUIT

A conventional UHF rectifier is based on Dickson Charge Pump. In CMOS process use diode-connected MOS take the place of diode, and two out-of-phase clocks is replaced by antenna amplitude. When GND is higher than RF_{in}, M1 is ON and C1 is charged. When RF_{in} is high, M1 turns OFF while M2 turns ON, the charge transfer from C1 to C2. To achieve high output voltage, multi-stage could be used. The output of an N stages Dickson's charge pump rectifier could be expressed as

$$V_{DC} = 2 \times N \times \left(V_{amp} - V_{th}\right)$$

(2)

Where N is the number of stages, Vamp is the amplitude of RF input signal, and V_{th} is the threshold of MOSFET. The diode-connect MOS can be represented as an equivalent resistance of resistor, and a single stage can be viewed as a RC network [3]. The delay of the stage could be expressed as

$$\tau = k \times R_{eq} \times C_c$$

(3)

Where k is the coefficient determined by the number of charge being transferred up to a proper percentage in a given period. With the frequency of clocks increased, the R_{eq} shows a significant effect of the power convert efficiency of the rectifiers. To decrease the resistances effect, various rectifiers scheme has been proposed [4][5]. Those methods can improve efficiency by reduce the R_{eq}.

3. PROPOSED DIFFERENTIAL-DRIVE RECTIFIER CIRCUIT

To achieve low on-resistance and small leakage current, the differential-drive CMOS rectifier has been developed. The rectifier's unit stage is shown in Figure 1, the cross-coupled differential configuration with a bridge structure is driven by a differential signal and the DC output is the source of the PMOS.

The basic operation of those four transistors is described in following. V_X and V_Y are complementary signal. When V_X is high and V_Y is low, the MP1 and MN2 are on meanwhile MP2 and MN1 are off, the V_{DC} equals V_X and the chassis ground (GND) equals V_Y. Therefore the output voltage is $2(V_{amp}-V_{th})$, where V_{amp} is the voltage amplitude of V_X (or V_Y), V_{drop} is the voltage drop cause by MOS resistance. For some applications, a high output voltage is needed. A multitude of stages could be series connected to get high voltage. The output voltage V_{DC} is decided by forward current, reverse current and current flowing through the load. With the steady-state assumption, the current consumed on load I_{LOAD} is equal to the charges transferred through the MP1 and MP2. The equation of I_{LOAD} as follows:

$$I_{LOAD} = \overline{I_{MP1} + I_{MP2}} = \frac{Q_{MP1} + Q_{MP2}}{T}$$

(4)

Where I_{MP1}, I_{MP2} is the current through pMOS, Q_{MP1}, Q_{MP2} stand for the charges flowing through pMOS during the period T. The mainly analysis (take MP1 as an example) is shown as follows:

When V_{gs} of MP1 increases, the MP1 start to conduct and work in saturation region. The current is as follows:

$$I_{sat} = K' \frac{W}{2L}\left(V_{gs} - V_{th}\right)^2 \left(1 + \lambda V_{ds}\right)$$

(5)

When the absolute value of V_{gs}-V_{th} decreases, MP1 work into linear region. The current is as follows:
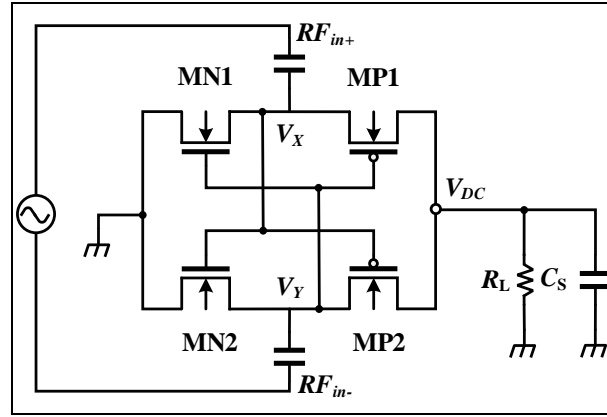
Figure 1. The proposed rectifier in this paper.

$$I_{linear} = K^{'} \frac{W}{2L} \left(V_{gs} - V_{th} - \frac{1}{2} V_{ds} \right) V_{ds} \qquad (6)$$

When the transistors operate in weak-inversion region, lead a low PCE because of the higher channel resistance. The weak sub-threshold current is as follow:

$$I_{sub} = I_{s0} \left[1 - \exp\left(-\frac{V_{ds}}{V_t} \right) \right] \exp\left(\frac{V_{gs} - V_{th} - V_{off}}{nV_t} \right) \qquad (7)$$

Where I_{s0} is given by

$$I_{s0} = \mu_0 \frac{W}{L} \sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}} V_t^{\,2} \qquad (8)$$

When the value of V_{gs} and V_{ds} is down to 0, the transistor enters the cutoff region. Due to the leakage current existence, maximum PCE cannot be achieved. The leakage current can be defined by:

$$I_{leak} = I_{s0} \left[1 - \exp\left(-\frac{V_{ds}}{V_t} \right) \right] \exp\left(\frac{-V_{th} - V_{off}}{nV_t} \right) \qquad (9)$$

By combining the above-described equations, the output voltage can be represent as a function three variables:

$$V_{out} = f\left(\frac{W}{L}, R_L, V_{th} \right) \qquad (10)$$

In N-stage rectifier, if we define the output voltage the Nth stage by V_{outN}, the output voltage can be solved by adding each stages

$$V_{out} = V_{out1} + V_{out1} + ... + V_{outN} \qquad (11)$$

The N-stage rectifier's power convert efficiency is computed as

$$PCE(\%) = \frac{P_{DC}}{P_{input}} \times 100 = \frac{P_{DC}}{P_{DC} + N \times P_{LOSS}} \times 100 \qquad (12)$$

Where P_{input} is the power received from antenna, P_{DC} is the rectifier's output power, the P_{LOSS} is given by

$$P_{LOSS} = P_{sat} + P_{linear} + P_{sub} + P_{leak} \qquad (13)$$

Where the P_{sat}, P_{linear}, P_{sub}, P_{leak} is the power dissipation at separate region of transistors.

The conversion efficiency does not take impedance mismatch into consideration, therefore it directly reflect the performance of the rectifier circuit rather than whole system. We use the circuit's efficiency as the main performance metric in this paper.

4. DESIGN AND CIRCUIT PERFORMANCE

A test chip was designed and fabricated with 0.35μm standard CMOS process. Figure 2 shows the micrograph of the fabricated test circuit, the active area is140μm*60μm not including the pad. The rectifier is compatible with standard CMOS processes. A conventional rectifier is fabricated as well. The off-chip series inductor is added to resonate out the input capacitance of the circuit. It provide Q voltage boosting and it presents a higher voltage at the input port of the rectifier to achieve a better efficiency. The low-loss probing pads is essential to avoided substrate loss.
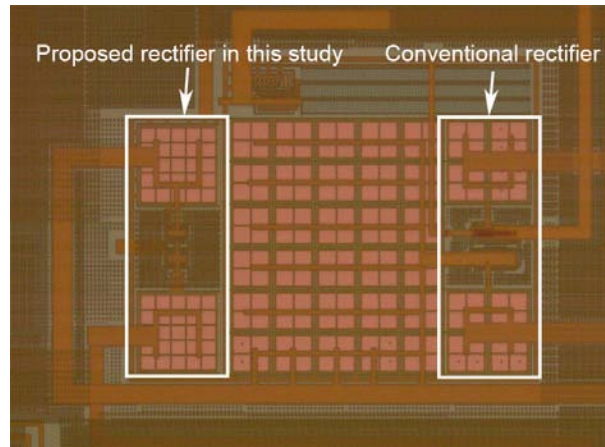

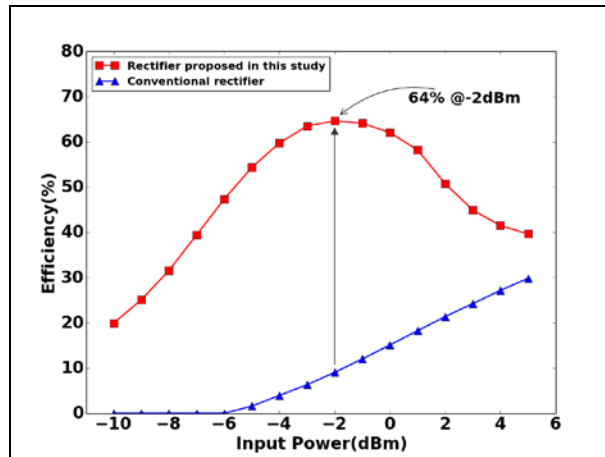Figure 2. Micrograph of the fabricated circuits

Figure 3. RF-DC converter efficiency versus the RF input power with different rectifier structure.
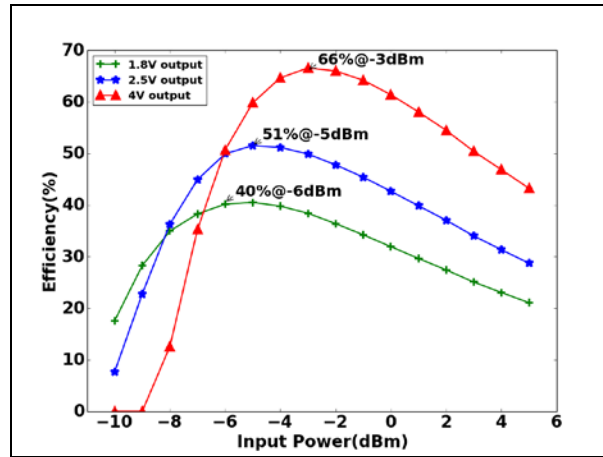
Figure 4. RF-DC converter efficiency versus the RF input power with different output DC voltage.

Table I. Performance Summary of CMOS UHF RF/DC Rectifiers

	This Work	**[6]**	**[7]**	**[8]**	**[9]**
Process	0.35μm standard	0.18μm	65nm RF	0.35μm FeRAM	0.25μm SOS
Stages	5	24	5	1	\
Frequency(MHz)	915	900	900	953	915
Pin(dBm)	-3	-11	+18	-3.5	-4
PCE(%)	66	26.50	31.80	42	71.50

The size was selected carefully for the balance between low equal on-resistance and low leakage current, therefore the width should be wide enough to achieve the proper I_{ds}. A smoothing polysilicon-polysilicon capacitor were placed at the output of the rectifier. The conventional CMOS rectifier were also fabricated with the same stages as the rectifier we proposed in this paper.

Figure 4 illustrate the PCE of both rectifier during sweep the input power from -10dBm to 5dBm at 915MHz with different loads. As shown in this figure, the maximum RF-DC PCE of the rectifier for a DC output power of 162μW (2.5V and 64μA) is about 51.5% at -5dBm input power. To provide high voltage for stimulator output, the maximum efficiency for a DC output voltage of 4V is about 66% at -3dBm. For large input power, a large DC output voltage can be produced. It is noted that the output voltage exceeds breakdown voltage might lead a permanent damage to the devices unless high-voltage devices is used at the output. The performance of this chip is summarized in Table I [6]-[9] and the comparison between this work and some of the state of the art works is also presented.

5. CONCLUDE

We developed a high-efficiency CMOS rectifier circuits for wireless power neural tissue stimulator. The analytic expressions for the output voltage and power conversion efficiency were presented by reasonable approximations. The differential-drive architecture can reduce the effective threshold voltage of diode-connected MOS transistors and it is proved that the proposed circuit has a better performance of the PCE compare to the conventional rectifiers. An available DC power of at least 200μW is generated by the CMOS rectifier at a RF input power of -4dBm. In comparison with the conventional rectifier fabricated with same process the efficiency has been enhanced significantly.

6. ACKNOWLEDGMENTS

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