# High-Precision Synchronized Pulse Generation for Mobile Multistatic Radar System

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*Abstract*—**In order to settle the problem of time and frequency synchronization of Mobile Multistatic Radar System (MMSRS), an algorithm that combines pseudo-noise (PN) code ranging and dynamic fine phase shift capability of Digital Clock Manager (DCM) module in FPGA is proposed to realize accurate synchronized pulse generation in high-dynamic environment. This method is presented by detailed principle and formula analysis. According to the simulation and experiment results, the synchronized deviation of our method using system clock of 80 MHz can reach within 0.30 ns, and the robustness of algorithm can be guaranteed as well. Besides, without the need of GPS, this method shows more benefits in military application.**

*Keywords—high-precision; synchronized pulse generation; Mobile Multistatic Radar System (MMSRS); high-dynamic*

## I.    INTRODUCTION

Mobile Multistatic Radar System (MMSRS) is a radar system consisting of distinct transmitters and receivers that are placed on separate motion platforms, e.g. aircraft, shipboard and missile. Due to its strong viability and flexibility of target detecting, MMSRS shows lots of potential advantages in modern communication war [1]. However, the system complexity and application environment of MMSRS leads to some technological challenges especially lying in synchronization of the system. The deviation of individual clock source and Doppler frequency shift caused by dynamic stress makes it a harsh task to generate unified high-precision synchronized pulse [2]. To overcome this problem, three synchronization methods have been figured out by some pioneer studies [3] [4]. Although those methods provide strengths in the improvement of synchronized precision and efficiency, most of them are still in the theoretical analysis and simulation period. What's worse, the anti-dynamic capability of radar has not been promoted effectively yet.

In order to enhance the anti-dynamic performance of MMSRS, some experts have made attempt to introduce the technique of pseudo-noise (PN) code ranging in radar system and provided a new strategy [5][6]. Over the past decade, a considerable amount of research on such scheme has been done, and provided some interesting and novel results. In the procedure of PN code ranging, code and carrier synchronization is the key of increasing synchronized precision and reducing time consumption [7]-[10]. Transmission delay can be measured precisely, which is the basis of sampling offset estimation. Furthermore, due to the periodic nature of PN code, the digital realization using sub-sampling technique can be designed based on FPGA, so the accurate adjustment of synchronized pulse can be realized by Digital Clock Manager (DCM) module in FPGA [11]. Thus, this paper addresses an algorithm of synchronized pulse generation based on PN code ranging, which is utilized to provide strict clock reference for MMSRS in high-dynamic environment. The core of it is to combine PN code ranging with dynamic fine phase shift capability of DCM module.

Following this section, the rest of the paper is organized as follows. Section II introduces the theory of PN code synchronization. In Section III, our proposed method is introduced in detail with principle diagram and formulas. The test results of the properties for this algorithm are shown in Section IV. Finally, Section V gives a brief conclusion.

## II.    THE TECHNNOLOGY OF PN CODE SYNCHRONIZATION

Employing PN code ranging algorithm in the design of MMSRS is one of the most important application of direct sequence spread spectrum (DSSS) in military communication system. As the basis of PN code ranging, PN code synchronization is the process of estimating the time delay between the received signal and its local replicas, which plays a vital role in the procedure of demodulation and dispreading. In this section, a brief introduction of PN code synchronization will be given, including the block diagram and the algorithm analysis.

### A.    the System Block Diagram of PN Code Synchronization

PN code synchronization is implemented by acquisition and tracking. The block diagram is shown in Fig. 1.

For a binary phase shift keying (BPSK)-modulated DSSS system, the model of received signal can be written as

$$r(t) = s(t,\tau) + n(t) \qquad (1)$$

where $s(t,\tau)$ is the transmitted signal and $n(t)$ is additive white Gaussian noise (AWGN). $s(t,\tau)$ can be expressed as

$$s(t,\tau) = \sqrt{2P_s}\, d\big((1+\xi)(t-\tau)\big) c\big((1+\xi)(t-\tau)\big) cos\big((\omega_{IF}+\omega_d)t+\varphi\big) \qquad (2)$$

where $P_s$ is the signal power, $d(t)$ is information code of bit rate $R_b$, while $c(t)$ is PN sequence of length $N$ and chip rate $R_c$. $\tau$ is the time delay normalized to the chip duration $T_c$ ( $T_c = 1/R_c$ ), $\omega_{IF}$ is the angular frequency of intermediate-frequency (IF) carrier and $\varphi$ is its initial phase. $\xi$ and $\omega_d$ denote for the dynamic parameters of signal and carrier. As such, the ultimate purpose of PN code synchronization is to estimate $\tau$, $\xi$, and $\omega_d$.

### B. Algorithm Analysis of PN Code Synchronization

#### 1) FFT acquisition algorithm

In high-dynamic environment, the data acquisition speed is of great significance, thus we choose the algorithm based on fast Fourier transform (FFT). The principle of it is to convert correlation process in time domain into multiplication process in frequency domain, i.e.

$$z(n) = \sum_{m=0}^{N-1} x(m) y(m-n)$$
$$= IFFT\left\{ FFT(x(n)) \cdot \overline{FFT(y(n))} \right\} \qquad (3)$$

where $x(n)$ and $y(n)$ represent the two sequences participating in the conjugate multiplier, while $z(n)$ is the normalized correlation result of $x(n)$ and $y(n)$. At last, the code and carrier acquisition is conducted by threshold comparison of the correlation result. Through FFT, fast correlation process can be overtaken, which is beneficial for the algorithm to shorten process time. Additionally, by phase shift in frequency domain, it helps to compensate for Doppler frequency offset effectively.

#### 2) Code tracking algorithm by DDLL

Code tracking is the procedure following code acquisition so as to make more precise estimation of the Doppler shift and code phase, which is carried out by Digital Delay-Locked Loop (DDLL), and the structure is shown in Fig.1.

The noncoherent early minus late power discriminator is used to detect the code phase deviation between $s(t,\tau)$ and its local replicas. The output is transmitted to the loop filter to calculate the frequency turning word (FTW). The DDLL adjusts FTW

through negative feedback so that the code rate of local replicas can be controlled. At last, the code phase is up-dated to make the locally generated code synchronized with the received signal.

Note that the principle of carrier tracking by carrier tracking loop is similar with that of code tracking, so due to the length limitation of this article, it is unnecessary to go into details.
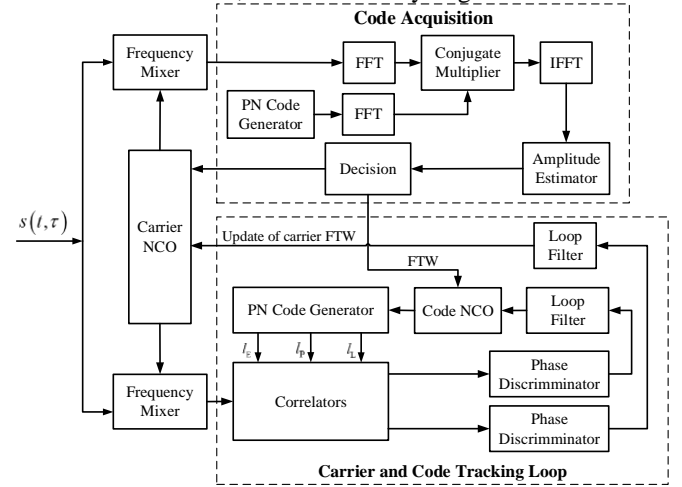


Figure 1. Block diagram of PN code synchronization

### III. PROPOSED SYNCHRONIZED PULSE GENERATION METHOD

In MMSRS, we assume one radar station to be the main station (MS), which builds data link with every other station separately, while the other ones, assumed to be secondary station (SS), only contact with the MS. The architecture diagrams of MS and SS are shown in Fig.2. The difference of the two stations' function is that the MS mainly takes the charge of ranging while the SS pays more attention to adjust its synchronized pulse according to the received ranging information.

### A. the Ranging Principle

The pseudorange is measured via estimating signal transmission delay between MS and SS. The technology of Self-Transmitting and Self-Receiving (STSR) ranging is a common algorithm of PN code ranging, whose principle diagram is displayed in Fig.3.

Since the clock sources are diverse among different stations, both MS and SS build individual time system according to their own time reference. As is shown in Fig.3, $t_M$ and $t_S$ denote for the moment recorded on the MS and SS respectively. The MS sends ranging frame at $t_{M1}$, and records the sending moment. When the SS receives the frame, the locally produced code which carries the dynamic information of the received signal will be transmitted back to the MS immediately, and the receiving moment is recorded as $t_{M2}$. A constant $T_d$ stands for the inner processing period of SS. Since $t_{M1}$ and $t_{M2}$ are both recorded referring to the clock system of MS, the transmission delay between the two stations can be easily calculated by

$$T_{\text{tran}} = \frac{1}{2}\left[\left(t_{\text{M2}} - t_{\text{M1}}\right) - T_d\right] \tag{4}$$

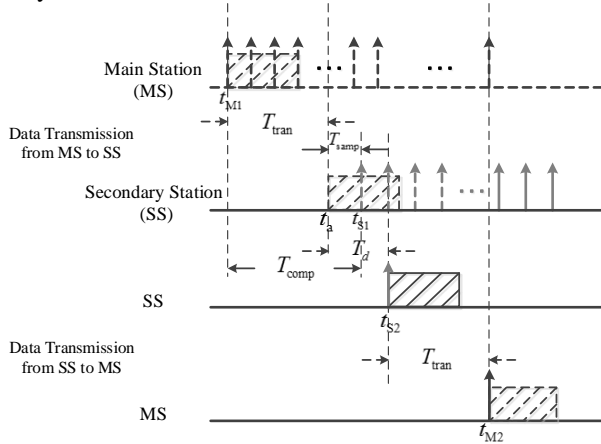In this way, the signal transmission delay can be measured precisely.



Figure 3. Principle diagram of STSR ranging

### B. the Proposed Sychronized Pulse Generation Algorithm

Review Fig.3 and we find that in the light of different clock sources, the SS is unable to sample the time of arrival ($t_a$) exactly, which leads to a sampling offset represented by $T_{\text{samp}}$. As such, the compensation value of synchronized pulse is

$$T_{\text{comp}} = T_{\text{tran}} + T_{\text{samp}} \tag{5}$$

In high-dynamic environment, $T_{\text{comp}}$ is affected not only by the clock deviation, but also by dynamic stress. Thus, care must be taken in design to real time estimate $T_{\text{comp}}$.
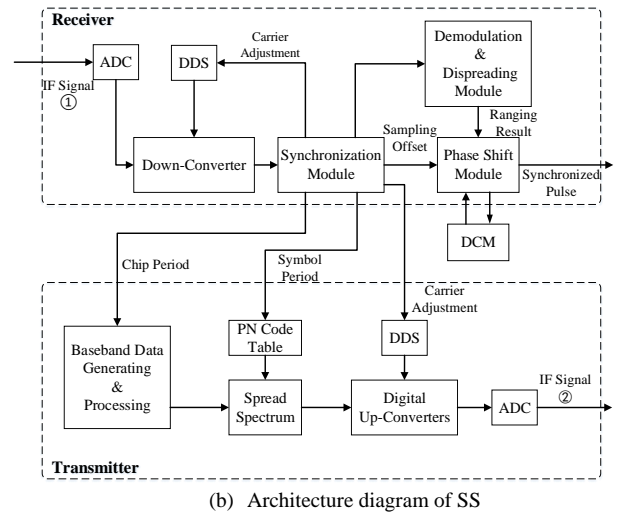
Theoretically, as long as the sampling pulse is output in the advance of $T_{\text{comp}}$, we can success generate the pulse synchronized with the MS; nevertheless, it is difficult to realize advance compensation, so we use delay compensation in practice. The principle diagram of our proposed algorithm is indicated in Fig.4, and the steps of such algorithm are shown as follow:

- Advance the starting moment of process for a constant period $T_{\text{pre}}$. The interval from $t_{\text{process}}$ to $t_{\text{S1}}$ is requested be longer than the maximum compensating time but shorter than a code period, i.e. $\left(T_{\text{comp}}\right)_{\max} < T_{\text{pre}} < N \cdot T_c$. Seen from Fig.4, the period $T'_{\text{comp}}$ between $t_{\text{process}}$ and $t_{\text{M1}}$ is the real compensating delay in our algorithm.

- Estimate $T_{\text{samp}}$. Before calculating $T'_{\text{comp}}$, we need to estimate $T_{\text{samp}}$. The code look-up table in DDLL is addressed by a 42-bit address signal: the 10-bit binary data of [41:32] stand for the integral part of the code phase, and the 32-bit data of [31:0] for the fractional part, so the estimation of $T_{\text{samp}}$ can be expressed by initial sampling phase of the corresponding addressing circulation. Assume the $k^{\text{th}}$ initial sampling phase is $P_k$, then the $(k+1)^{\text{th}}$ sampling offset is

$$P_{k+1} = \left(P_k + \left\lceil\left(N \cdot 2^{32} - P_k\right)\big/\Delta P_k\right\rceil \cdot \Delta P_k\right)\%2^{32} \tag{6}$$
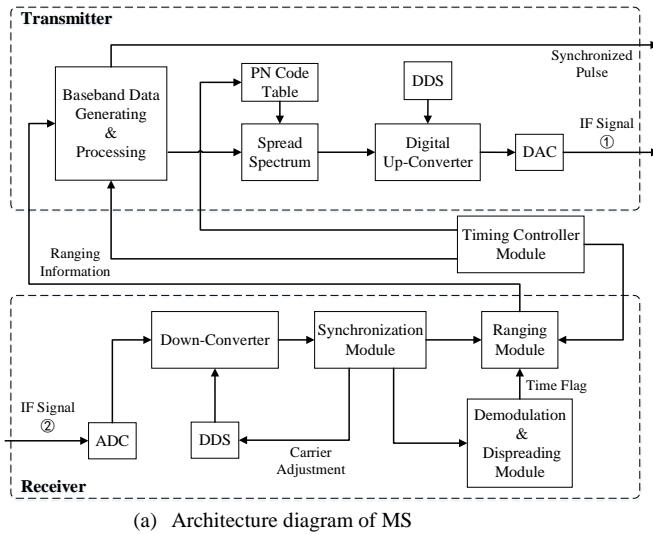


(a) Architecture diagram of MS      (b) Architecture diagram of SS

Figure 2. Architecture diagram of the whole system

where $\Delta P_k$ represents the k$^{th}$ FTW of local code generator and $\lceil \square \rceil$ means round to the nearest integer towards infinity. Then the $(k+1)^{th}$ initial sampling shift $T_{samp(k+1)} = P_{k+1} / (R_c \times 2^{32})$, which equals $T_{samp}$.

- Estimate $T'_{comp}$. From Fig.4, considering the dynamic estimation is mainly related to the relative velocity and acceleration, we can get $T'_{comp}$ by

$$T'_{comp} = T_{pre} - T_{comp}$$
$$= T_{pre} - T_{samp} - T'_{tran} - \frac{1}{c}\frac{\partial R}{\partial t}(N \cdot T_c) - \frac{1}{2c}\frac{\partial^2 R}{\partial t^2}(N \cdot T_c)^2 \quad (7)$$
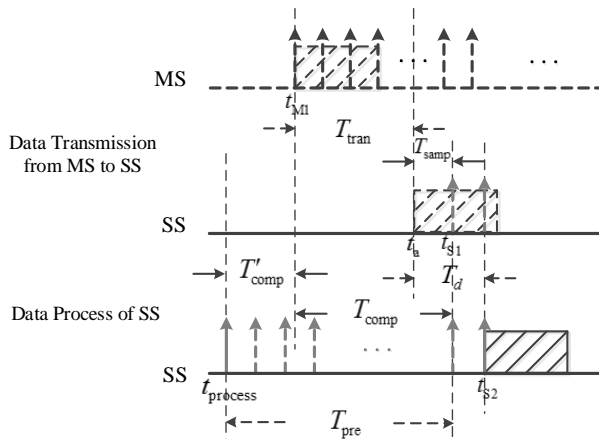


Figure 3.   Principle diagram of the proposed algorithm

where $T'_{tran}$ represents the prior result of transmission delay got at ( $t_{S1} - N \cdot T_c$ ), $c$ is speed of light, and ($\partial^n R / \partial t^n$) denotes for dynamic parameter, which can be estimated through ranging. Besides, attention must be paid that $T'_{tran}$ may not be integral multiple of clock period, so the fractional part needs to be presented by code phase.

- Calculate the integral and fractional part of $T'_{comp}$ through:

$$N_{int} = \left\lfloor T'_{comp} / \left(R_c / f_{clk} \times 2^{32}\right) \right\rfloor \quad (8.1)$$

$$N_{frac} = T'_{comp} \% \left(\left(R_c / f_{clk}\right) \times 2^{32}\right) \quad (8.2)$$

where $f_{clk}$ is the system clock rate of SS, and $\lfloor \square \rfloor$ means round towards minus infinity.

With the correction of $N_{int}$ by counting the number of clock period, the deviation of the synchronized pulse can be reduced within one clock period. To increase the precision of synchronized pulse, a further procedure must be introduced to accomplish accurate compensation of $N_{frac}$, which is also described by code phase.

- Compensate for $N_{frac}$. Seen from Fig.2(b), the accurate phase adjustment is carried out by DCM module in FPGA, which can be easily configured using IP core generator. Based on phase-locked technique, DCM is able to provide the function of digital phase shifter, whose precision can reach to $1/256$ of a clock period.

After $\quad M = \left(N_{frac} / \left(\left(R_c / f_{clk}\right) / 2^{32} \times (1/256)\right)\right) \quad$ times procedure, the SS is managed to generate high-precision synchronized pulse with the same precision level as the order of system clock, which is used for the flag of time and frequency synchronization.

## IV.   THE RESULTS AND ANALYSIS

In our numerical analysis, we consider a DSSS system with the parameters set as follow: BPSK Modulation, $R_b = 10$ Kbps. The Carrier Noise Ratio is $CNR = 70$ dB$\cdot$Hz. A PN code of $N = 1023$ and chip rate $R_c = 10.23$ MHz is sampled at $f_s = 80$ MHz . The maximum Doppler Frequency is $f_d = 20$ KHz . The algorithm simulation is conducted by MATLAB, and the digital realization of the proposed method is written in Verilog coding and tested on Xilinx FPGA XC5VSX95T.

Firstly, the feasibility analysis of our algorithm is given by the simulation of PN code ranging error under the condition that ( $\partial R / \partial t$ ) is $200$ m/s , as is shown in Fig.5 and Fig.6. The line in Fig. 5 represents the real distance value, while the points stand for the measuring results. Apparently, the measuring results fluctuate in the vicinity of the real value, and the deviation is illustrated in Fig.6 more directly. The standard deviation of ranging is 0.034 ns . Thus, the presented algorithm has the potential ability to meet the requirement of high-precision in MMSRS.
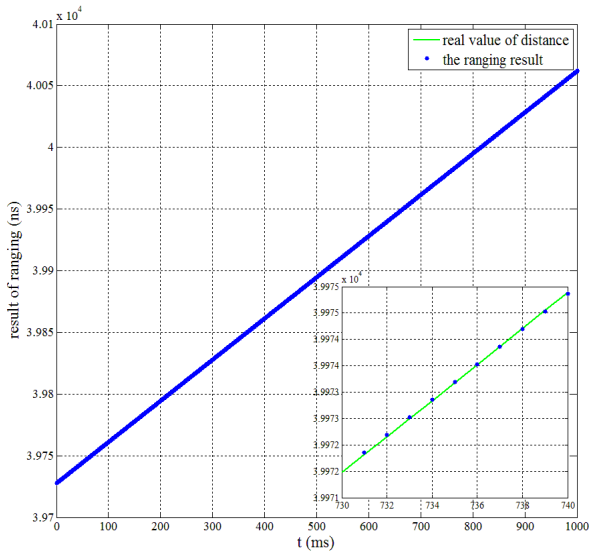
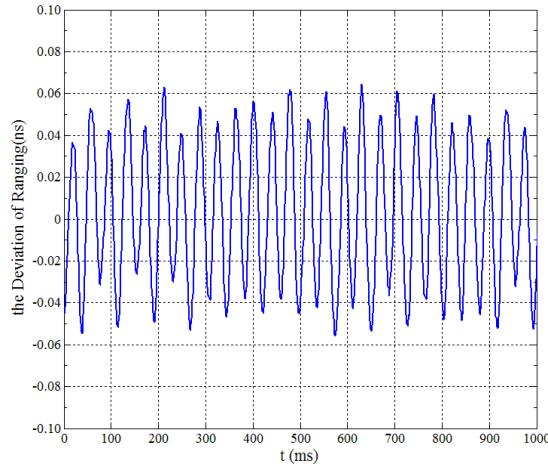Figure 4. Distance measuring results when $\partial R/\partial t = 200$ m/s



Figure 5. Deviation curve of distance measuring result when $\partial R/\partial t = 200$ m/s

In the performance test for the FPGA implementation, the dynamic parameters are added into the signal by signal emulator. The statistic results are observed through oscilloscope Agilent InfiniiVision MSO-X4104A. Fig.7 indicates the synchronized pulses of the three stations when $\partial R/\partial t = 200$m/s . The first wave stands for the synchronized pulse of MS, while the other two are produced in the two SSs. As can be seen, the three pulses appear almost at the same time, and the result is consistent with the theoretical analysis above.

Then we further expand the setting of dynamic parameter to be $\partial R/\partial t = 0, 100, 200$ m/s . For each condition, two groups of tests for 1 hour and 8 hours separately are conducted. We repeat both of the two groups for 500 times totally and at last calculate the statistical average as the final results, which are shown in Table. I. As can be seen, in the static state ( $\partial R/\partial t = 0$ ), the precision of synchronized pulse is within $0.25$ ns . When ( $\partial R/\partial t$ ) changes from 0 to $200$ m/s , the standard deviation of pulse offset is still less than $0.30$ ns .This deviation is lower than $2.4\%$ of the resolution of a clock period ( $12.5$ ns ) and the effect of the increase in velocity can be alleviated. In addition, comparing the results of the two lines, it can be figured out that as time passes, there is no evident decrease in the synchronized precision, which confirms the robustness of algorithm.
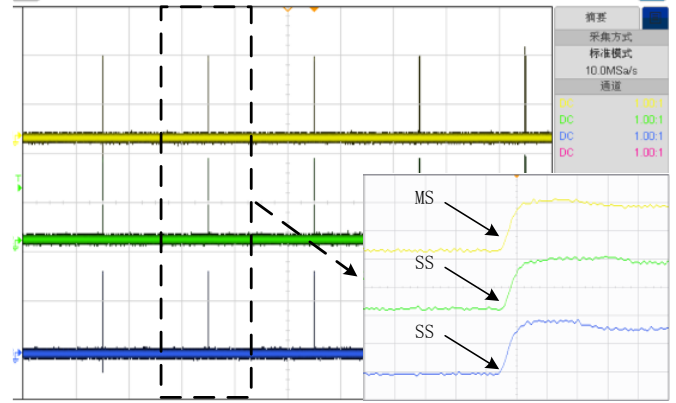


Figure 6. Observation result of the synchronized pulse in actual environment

## V. CONCLUSIONS

In this paper, an algorithm of high-precision synchronized pulse generation for MMSRS is proposed. The principle analysis and FPGA implementation architecture are discussed in detail. The key of our new method is to combine PN code ranging with dynamic fine phase shift capability of DCM module in FPGA so that the pulse offset introduced by dynamic stress and clock deviation can be compensated for accurately. The simulation and experiment results confirm its properties of high precision and strong robustness of algorithm. The application of this novel technology for MMSRS can be spread in the design of aircraft and missile. What's more, without the usage of GPS, our method shows more extensive application prospect in military field.

TABLE I. TEST RESULTS OF DIFFERENT RELATIVE VELOCITY

| $\partial R/\partial t$ (m/s) | 0 | | 100 | | 200 | |
|---|---|---|---|---|---|---|
| Test Period (hour) | Standard Deviation of Ranging (ns) | Standard Deviation of Pulse Offset (ns) | Standard Deviation of ranging (ns) | Standard Deviation of Pulse Offset (ns) | Standard Deviation of Ranging (ns) | Standard Deviation of Pulse Offset (ns) |
| 1 | 0.03 | 0.22 | 0.04 | 0.21 | 0.04 | 0.24 |
| 8 | 0.04 | 0.25 | 0.04 | 0.27 | 0.04 | 0.28 |

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