

The Influence of Source Charge collection and Parasitic Bipolar Effect on 65nm Single Event Transient Pulse Width

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Abstract. The parasitic bipolar conduction in CMOS source-well-drain structure triggered under heavy ion irradiation will cause wider pulse width. The source, commonly though the emitter, will inject charge to the well, so that the drain has to collect additional charge and create a wider pulse. However, in our study, the source may inject charge through parasitic bipolar conduction, but the source will also collect charge through drift and diffusion meanwhile. Under proper well contact, the charge collected by the source will exceed the charge injected by the source, resulting in a narrow pulse. Compared with NMOS, the n-well potential of PMOS tend to be disturbed easily, therefore parasitic bipolar will get conducted easily and more attention need to be paid to PMOS.

Introduction

As technology scales down to nanometer, Single Event Transient (SET) has exceeded Single Event Upset (SEU) and become the main source of circuit soft errors [1]. SET pulse width, the most important factor of an SET, determines whether the pulse will propagate, get caught or not. Parasitic bipolar plays an important role in the SET pulse width. Study has shown the parasitic bipolar conduction occurs under heavy ion irradiation will result in drain additional charge collection and cause a wider pulse [2-4]. Reference [3] simulates the pulse width using devices with and without the source implant(i.e., with and without the emitter junction for the parasitic bipolar transistor), results show device with source will collect more charge due to parasitic bipolar effect, which lead to a wider pulse. P-well voltage variations caused by an ion strike are much smaller than the n-well since the connection of p-well to the p-substrate provides effective control of the p-well potential. Therefore PMOS devices show high parasitic bipolar amplification compared with the NMOS device due to a voltage perturbation in the n-well during the charge collection process, so the pulse width of PMOS tends to be wider than NMOS [5]. Frequent well contacts has been proved to effectively mitigate the parasitic bipolar effect [6][7]. As the technology scales down, the feature size of device scales down and the critical charge for a node to form a pulse reduces, but the charge created by heavy ions and the area one heavy ion affects do not reduce in the same proportion. Other factors, such as temperature [8][9], supply voltage [9], have been proved to have influence on pulse width. So the charge collection becomes more complicated after heavy ion hit as technology scales down. In our simulation, the source collects charge through drift and diffusion besides injecting charge to well through parasitic bipolar conduction. The charge collected by the source exceeds the charge it injected in the case of proper well contact, and can shorten SET pulse width.

Simulation setup

The 65nm 3-D TCAD models used for the simulations were modeled and calibrated to match the electrical characteristics of SMIC 65nm spice model. One of the 65nm TCAD models is shown in Fig. 1. The electrical characteristics such as I_D-V_G and I_D-V_D of both PMOS and NMOS are shown in Fig. 2.

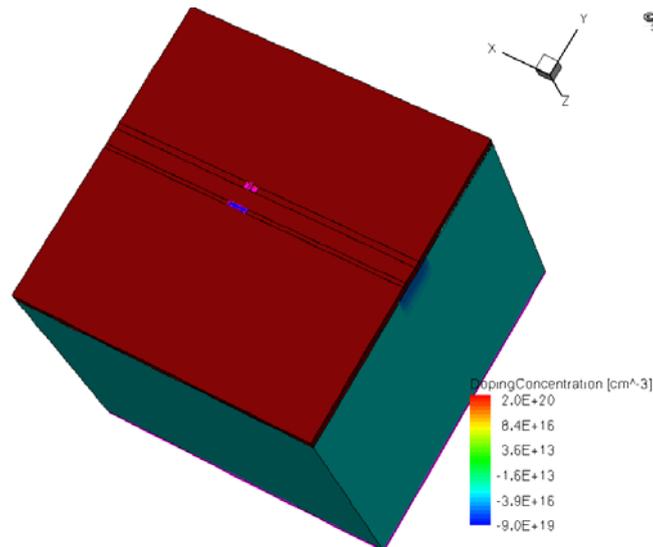


Fig. 1 3-D TCAD model used for mixed-mode simulation

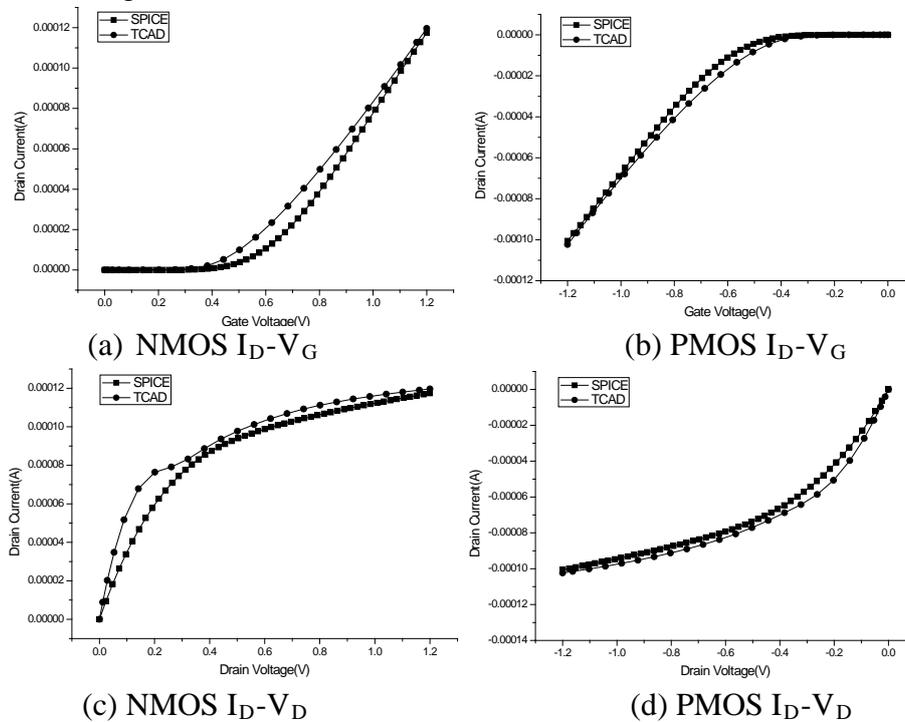


Fig. 2 Electrical characteristics calibration of TCAD model

All simulations are a mixed-mode setup of an inverter chain. The target devices were implemented with TCAD model while the others were using spice compact models. The current transient and voltage transient of drain and source are simulated under different well contact size. Charge collection is recorded as the integrated current through the electrode. The influence of source charge collection is restricted by removing the source of the MOSFET. The p-n-p(n-p-n) structure is destroyed by removing the source electrode so the parasitic bipolar conduction is restricted, which means the charge collected by the drain is by drift and diffusion.

Simulation Result

The NMOS source current and drain current are shown in Fig. 3. As seen in Fig. 3(a), the current of source has only an electron current component and the hole current is negligible. The current of source is positive which indicates that the source helps collect electron. The drain current is shown in Fig. 3(b). The drain current has an electron current component and a hole current component. The electron current is positive while the hole current is negative. The electron current is caused by

electron drift and diffusion. Parts of the electron recombine with holes during this period, which is the origin of negative hole current.

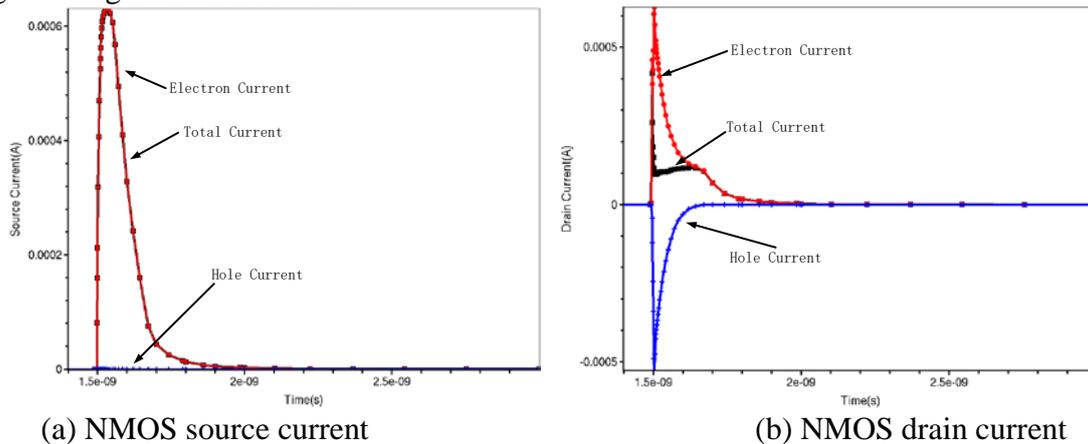


Fig. 3 NMOS current transient at LET=40MeV-cm²/mg

The PMOS source current and drain current are shown in Fig. 4. Different to NMOS, the current of PMOS source has both electron current component and hole current although the hole current component is much larger than electron current. Source current decreases gradually and stays positive for a while, which is the contribution of the parasitic bipolar conduction. The drain current is shown in Fig. 4(b). The drain current has a hole current component and an electron current component, too. The hole current is negative while the electron current is positive. The hole current is caused by hole drift and diffusion, and parts of the hole recombine in this period, which is the origin of positive electron current.

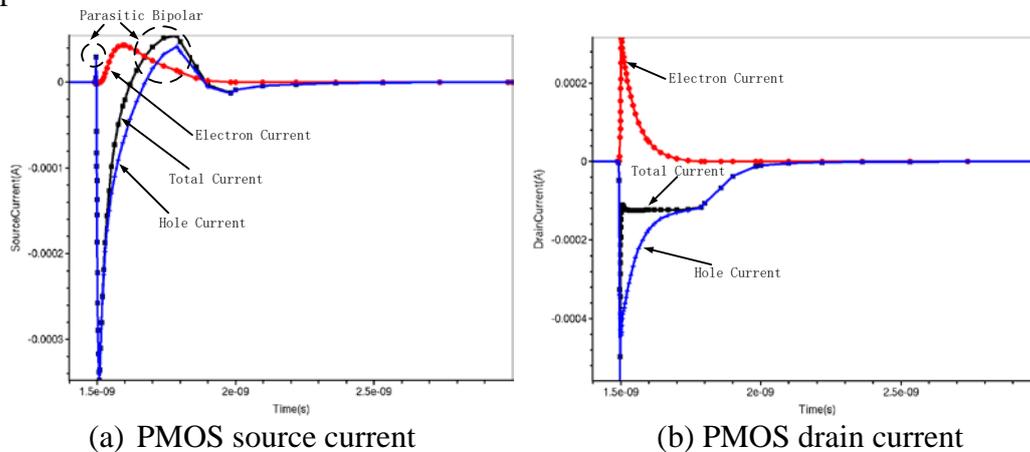
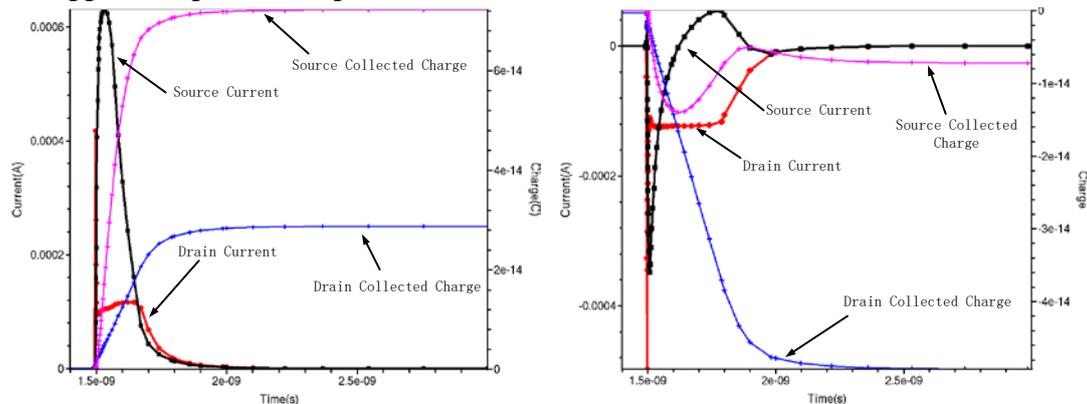


Fig. 4 PMOS current transient at LET=40MeV-cm²/mg

Drain current and source current are plotted in one figure to investigate the source charge collection. And we can figure out the direction of source current and drain current are the same, which indicates the main role of source is collecting charge. The charge collected by the electrode is recorded by the integration of current. As can be seen from Fig. 5(a), the charge collected by NMOS source is twice larger than the charge collected by NMOS drain. In the contrast, the source of PMOS collects little charge and the drain of PMOS collect more charge. The parasitic bipolar of NMOS is not triggered in this condition and the main role of the source is collecting charge and reducing the charge collected by the drain, which mitigate the SET at last. The technologies modeled have p-doped substrates and charge generated by an ion strike in PMOS is constrained in the n-well and thus the parasitic bipolar is prone to triggered. As seen in Fig 5(b), the parasitic bipolar is triggered with source injecting hole to the drain through source-well-drain path, and the drain collects a much larger amount of charge to form a wider pulse. Guess are made that the main role of source is collecting charge under proper well contact, and the charge collected by the source is much larger than the charge collected by the drain. But parasitic bipolar take control when the

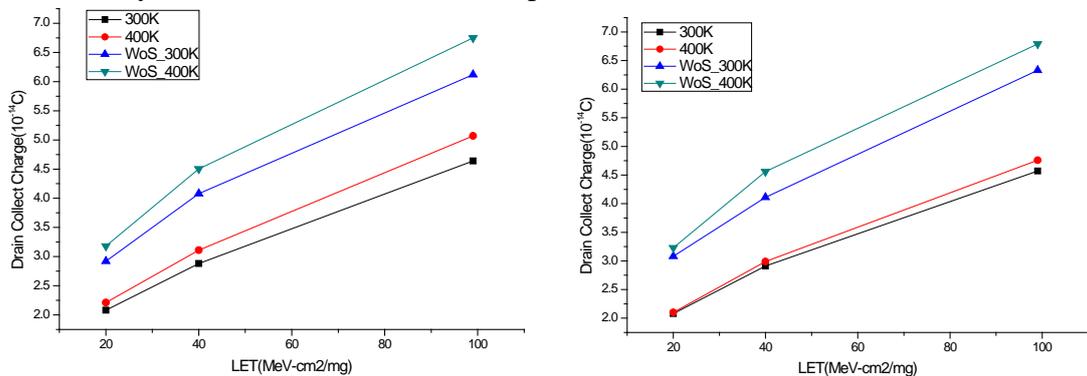
well contact area is not enough to prevent the device well potential from disturbance by heavy ion hit. In the simulation of PMOS, the charge collected by the source reduced sharply because the heavy ion triggers the parasitic bipolar conduction.



(a) NMOS current and collected charge (b) PMOS current and collected charge
 Fig. 5 Current transient and collected charge at LET=40MeV-cm²/mg

In order figure out the role of source charge collection at different well contact, we compared the charge collection of devices with and without source under different well contact size. Results are shown in Fig. 6 and Fig. 7. As shown in Fig. 6, the charge collected by the NMOS drain increases after removing the source of the devices at both well contact size and the SET pulse width is wider compared with the devices with source. This indicates that parasitic bipolar conduction does not triggered under both well contact size in NMOS and the main role of source is to collect charge. So the charge collected by drain increase after removing the source of the devices.

In PMOS, situation becomes a little different. The charge collection shows different characteristic at different contact size. When the contact size is small, the charge collected by the drain increases slightly after removing the source at low LET. The main reason is that charge deposited at low LET is small and the well potential varies little. High LET deposited enough charge and well potential varies, source injects hole to the well due to parasitic bipolar conduction, so the charge collected by the drain increases sharply in the devices with source. Source current also shows that on the one hand, the source collects charge, but on the other hand, the source injects charge through parasitic bipolar. When using large well contact area, the heavy ion hit does not trigger parasitic conduction and the source collects charge mainly. After removing the source, charge collected by the drain increases and SET pulse width increases.



(a) NMOS with small well contact (b) NMOS with large well contact
 Fig. 6 Charge collection of NMOS with and without source

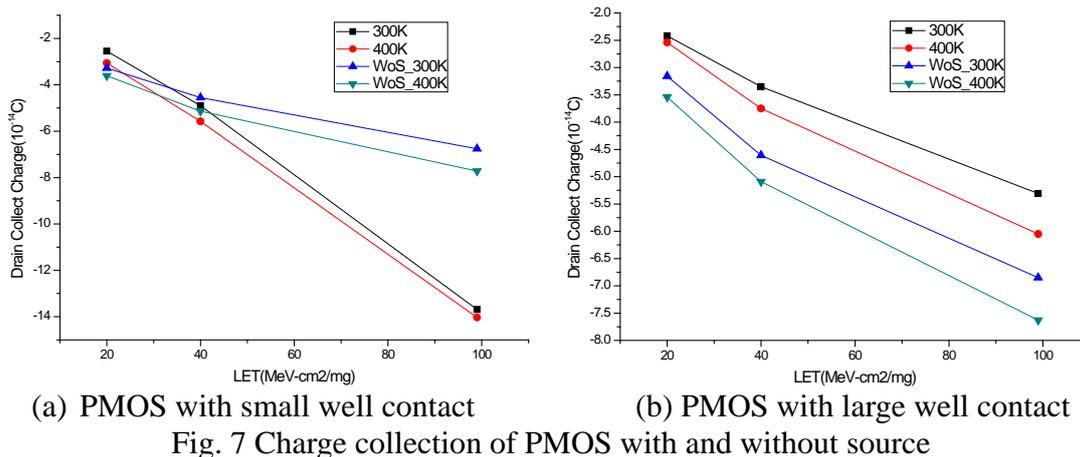


Fig. 7 Charge collection of PMOS with and without source

The connection of p-well to the p-substrate provides effective control of the p-well potential, so that small well contact size can insure the p-well potential and voltage variations caused by an ion strike are too small to trigger the parasitic bipolar conduction in NMOS. But PMOS n-well tends to disturb easily and need much larger well contact size to prevent the parasitic bipolar conduction. Compared the charge collected by the devices with and without source, we can figure out the source can help collect charge indeed. As shown in [2], the direction of drain current and source current are reversed in micron technology, in which the parasitic bipolar dominates the charge collection. In our simulation of 65nm technology, the direction of drain current and source current are the same, indicates the charge collected by the source exceed the charge injected from the source through parasitic bipolar effect. Meanwhile the source, acting as the emitter of the parasitic bipolar, injects charge to the well when well potential varies and parasitic bipolar conducts. So the drain collects additional charge and creating wider pulse when well contact is not enough. Increasing well contact size restrict the parasitic bipolar and reducing the SET pulse width.

Mitigation strategy

The parasitic bipolar effect plays an important role in charge collection and SET pulse width. For a single MOSFET, the drain will collect additional charge if the heavy ion strikes trigger the parasitic bipolar conduction. Proper well contacts should be used to prevent the parasitic bipolar from conducting. Simulations have shown that in 65nm twin well technology, the n-well potential disturbs more easily compared with the p-well potential. So the parasitic bipolar effect in PMOS is more serious than that in NMOS and the mitigation strategy need to treat PMOS and NMOS differently to insure SET hardness. When using proper well contact, the parasitic bipolar will not conduct and the role of the source is collecting charge. The extended source can be used to reduce the charge collected by the drain, and to reduce the SET pulse width.

Conclusion

The role of source in charge collection and parasitic bipolar effect on 65nm SET pulse width is analyzed through TCAD simulation. Under proper well contact, the charge collected by the source exceeds the charge injected to the well from the source. The main role of source is collecting charge in proper well contact and can reduce the SET pulse width. The potential of PMOS n-well are tend to be disturbed easily compared with the NMOS p-well in same well contact size. More attention should be paid to the mitigation of PMOS SET pulse width.

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