Trench based stress modulation structure for 90nm-gate CESL strained N MOSFET

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Abstract. A novel trench based stress modulation structure for strained 90nm-gate N MOSFET is demonstrated in this letter. The numerical simulation using SENTAURUS SPROCESS shows that, with this structure, the channel stress can be changed from compressive to tensile in a case of compressive CESL strained device. The relationships between the channel stress and the trenches' size are also investigated and it is deduced that the optimized trench depth and width can both be set to be 0.4um. With the trenches' size optimized, the trench based device can achieve an output current 24% higher than that of the N MOSFET without the trench based structure.

Introduction

In this paper a new optimal design of soccer robot control system which is based on mechanical analyses and calculations on the pressure and transmutation states of chip kick mechanics, this new control system with high precision for speed control and high dynamic quality. In last twenty years, strained Si technology has attracted much attention for it is regarded as a solution to improve Si MOSFET performance other than scaling down approach [1-3]. The basic idea of strained MOS is to enhance carriers' mobility in channel by making the semiconductor material there stained. There have already been various approaches to induce the channel stress, among which the stress liner technology has been widely investigated. With this approach, a strained SiN cap layer, which is called CESL (contact etch stop layer), is deposited on the device's surface to generate the stress [4-6]. However, while CMOS integrate circuit is considered, a single CESL cannot meet the requirement for that the strained P MOS and N MOS need compressive and tensile SiN cap layers respectively [6,7].This makes related fabrication process complicated.

Considering this, in our previous work [8,9], it has been demonstrated that, if a well designed trench based structure is introduced to modulate the channel stress, P MOSFET and N MOSFET can be improved by the same type CESL. In this letter, trench based structures for strained 90nm N MOSFET are considered and the effects of the trenches' geometric parameters on devices' channel stress are investigated in detail.

Device Structure

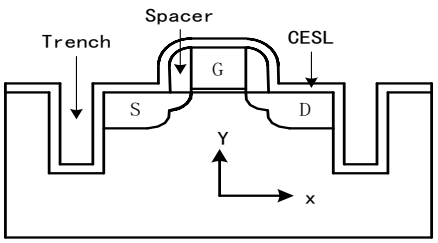


Fig.1 Cross section of the strained N MOSFET with a trench based structure.

Fig. 1 shows the device's structure. Being different from the conventional CESL strained MOSFET, there are two trenches beside the terminals of source and drain respectively. These trenches are not filled by insulator or any other materials, except for that the CESL layer is directly

deposited at the inner surface of them. This trench based structure can affect the channel stress significantly. The related mechanism can be found in our previous work [8, 9], and here we only give a brief explanation. In the case of a conventional CESL strained MOSFET which has no such trenches, the channel stress is dominated by the CESL beside, not on, the gate. Hence, a compressive CESL will induce a compressive channel stress. However, in the device demonstrated in fig. 1, the trenches can significantly weaken the CESL beside the gate and thus the CESL on the gate becomes dominant. As the result, a tensile channel stress can be induced by a compressive CESL, which seems much different from the case of a conventional CESL strained MOSFET.

In this letter, the CESL strained 90-nm gate N MOSFET is considered. All the calculations are done using SENTAURUS SPROCESS. The Typical parameters are adopted in the simulation, which are set as follows. The source length Ls and drain length Ld are both set to be 150nm. The thickness of gate is 30 nm. The thickness of CESL is 60 nm and the intrinsic stress in it is -2.5 GPa.

Results and Discussion

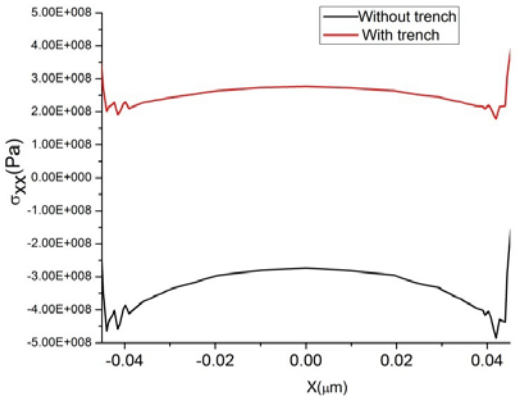
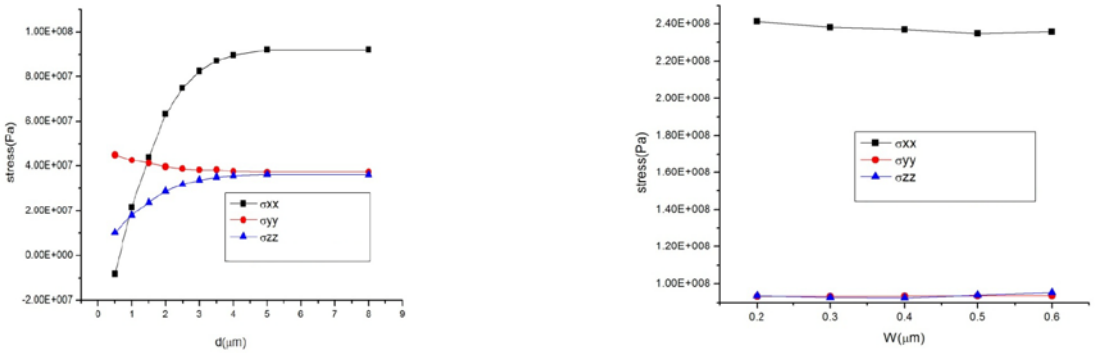


Fig.2 The distribution of the xx component of stress σxx in channel

Fig.2 shows the xx component of the channel stress of a strained MOSFET with the trench based structure as mentioned above. The width and depth of each trench are both 0.4um. For comparison, the simulation result of the conventional strained device with the same geometric and electronic parameters, but without the trenches, is also demonstrated in the same graph. It is observed that, the trench based structure successfully makes the channel stress change from compressive to tensile. In other words, the trench based structure works.

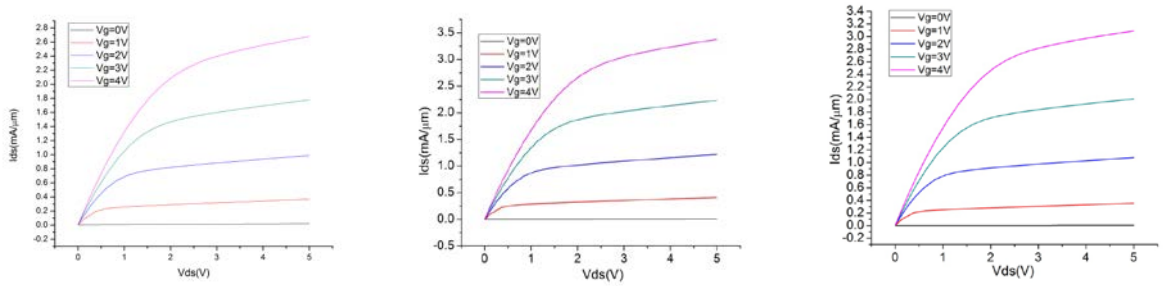


(a) (b)

Fig. 3 The dependence of the average channel stress on trench depth (a) and trench width (b)

Fig. 3 (a) shows the dependence of the average channel stress on trench depth, while the trench width is fixed to be 0.4um. It is observed that the xx component of the stress tensor σ_{xx} is dominant and hence the channel stress is almost uniaxial. It is also demonstrated that σ_{xx} increases with trench depth h and becomes saturated while being lager than 0.4um. Thus, 0.4um can be regarded as an optimized value of h in this case.

Fig.3 (b) shows the dependence of the average channel stress on trench width, while the trench depth is fixed to be 0.4um. It is observed that the channel stress is not closely related to the trench width. Considering the feasibility of the trench fabrication, trench width can be chosen to be any value larger than 0.2um.



(a) (b) (c)

Fig4 I-V output profiles of the trench based device (a), conventional strained device (b) and unstrained device (c)

The I-V output profiles of the trench based device are shown in fig. 4(a). The tensile stress in channel makes the electron mobility there enhanced, and thus improves the device performance. To demonstrate this, the I-V profiles of the conventional strained device (with a compressive CESL similar to that adopt in the trench based device) and the unstrained device are shown in fig. 4(b) and 4(c) respectively for comparison. It should be stressed that the conventional strained device here is degraded by the compressive CESL for that, in a general view point, the compressive CESL will induce a compressive channel and then reduce the electron mobility. However, this is not the case for our trench based device whose trenches can modulate the channel stress effectively. To demonstrate this more clearly, the transmit profiles of the three devices mentioned above are shown in fig. 5. It can be observed that the trench based device has the highest output current, which is 24% higher than that of the strained device without trenches.

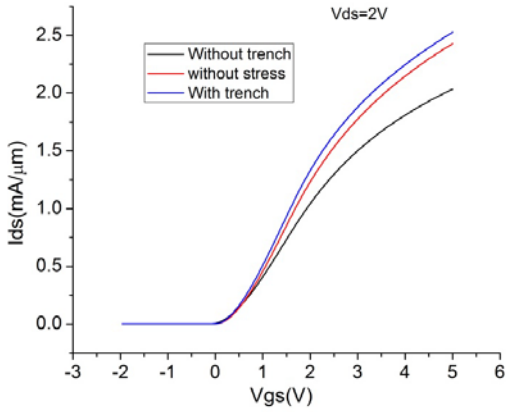


Fig. 5 The comparison of the transfer characteristic curves of the trench-based strained, the conventional strained and the unstrained device.

Conclusion

It is demonstrated that our trench based structure can effectively modulate the channel stress in strained N MOSFET. If it is properly designed, a tensile channel can be realized while the CESL cap layer is compressive, which seems non-intuitive in a traditional view. The numerical simulation using SENTAURUS SPROCESS shows that the effect of the trench based structure is positively related to the trench's depth, but not sensitive to the trench's width. For the typical 90nm-gate N MOSFET investigated in this letter, the optimized trench depth and width can both be set to be 0.4um. To get a deeper understanding of this stress modulation structure, further investigation needs to be done.

Acknowledgement

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