Double edge triggering technique for energy efficient server to reduce data center's impact on environment[*]

Jason McKneely

Electrical and Computer Engineering Department,
University of Alaska Fairbanks
Fairbanks, Alaska, USA
E-mail: jbmcneely@alaska.edu

Pei-Yi Zhao , Lun-Yao Wang, Yin- shui Xia and Ling-li Wang
E-mail: zhao@chapman.edu

Data centers worldwide have consumed massive amount of energy. The server processor energy efficiency has the biggest impact on energy usage in data center. In this paper, factors determining the processor circuit power are introduced and different power saving techniques are briefly reviewed. A novel methodology of using double edge triggering in server processor is proposed. By using the proposed double edge triggering implicitly pulsed CBS_ip flip-flop, the estimated energy saving of data center could be 4.3%; the energy saving on worldwide data centers will be estimated over 12 B kWh.

Keywords: Low Energy, Data center, Double Edge Triggering Flip-flop, Environment.

1. Introduction

Data centers are the information manufacturing centers that shape our modern experience. To satisfy the exploding needs of Big Data and Cloud Computing, the number of data centers have been significantly growing. However data center worldwide consumed massive amount of energy [1-4]. Data center electricity dissipation is projected to increase to roughly 140 billion KWH annually by 2020, equivalent to the annual output of 50 power plants, and emitting nearly 100 million metric tons of carbon pollution each year [3]. Data centers worldwide also contribute to 2% of global green emission which is equivalent to the green emission produced by 50 power stations. To reduce cost of removing excessive heat produced by data center, Microsoft tried an experiment called

Project Natick that put data center under the sea in early 2016; however the heat given off by the data center will seriously impact the natural habitat of the sea life. Some companies move data centers to areas close to Arctic Circle however it could melt ice berg in long term. Hence, saving energy in data center is extremely important environmentally and financially. Among areas identified for improvement in data center energy usage the processor energy efficiency has the biggest impact. There is a remarkable Energy Cascade Effect [6] in Data Centers: every Watt of saving that can be achieved on the processor level creates approximately 2.84 Watts of saving for the data center at a Power Usage Effectiveness (PUE) of 1.9. The Energy Logic Model describes that processor energy accounts for 15% of the total data center energy[11].Energy Star program by U.S. government suggested data centers to use processors that consume less power, more efficient power supplies, and cooling fans that are more energy-efficient, etc.[7].In the following sections, we first analyze factors determining power and then describe server processor power saving techniques and strategies. After that we will propose a double edge triggering methodology to save processor energy in data center.

2. Power Consumption Formula and Power Saving Technique

Power consumption of processor circuit is determined by several factors including frequency f, supply voltage V, data activity α, capacitance C, leakage, and short circuit current: $P = P_{dynamic} + P_{shortcircuit} + P_{leakage}$ where $P_{dynamic} = \Sigma \alpha * C * V2f$, $P_{shortcircuit} = I_{shortcircuit} * Vdd$, $P_{leakage} = I_{leakage} * Vdd$.

Dynamic power typically contributes a larger percentage of the processor power, particularly when the processor is running at a high utilization in high-power server CPU designs in data center. Based on the above factors, there are various ways to lower the power consumption of processor, for example, reduction of switching activity, reducing voltage, and changing frequency.

2.1. *Reduction of switching activity*

One way to save power of processor is to reduce switching activity, for example, turn the processor off when possible. There are two ways to turn it off: clock gating and power gating. Clock gating is a widely used method of stopping the clocks to a given block of logic to reduce dynamic power [1] when the input remains unchanged. Another method is power gating which removes all power from a circuit that saves both leakage and dynamic power. Power gating removes all power so that leakage power is also driven to zero. State is lost with power gating, so special method (like using state retention flip flop) must be used in conjunction with power gating.

2.2. *Dynamic voltage management*

Another way to reduce energy is to scale voltage, which is to lower the voltage, without significant performance degradation when the system has low work load. Voltage has quadratic relation with power because of equation P=$\Sigma\alpha$*C*V2f. Reduce voltage can reduce power effectively.

2.3. *Changing frequency*

The third way to save energy is to change frequency when work load is low and high performance is not required, or to use double edge clock triggering which can decrease the clock frequency to half. We propose a methodology of using double edge triggering in the next section.

3. Novel Double Edge Triggering Methodology to Save Power in Data Center

The clock system, which consists of the clock distribution network and sequential elements (flip-flops and latches [8-10]), is one of the most power consuming components in processors. And the clock system may account for 50% of the total dynamic power dissipation in processors in high performance servers. Currently the servers in data center worldwide employ single edge trigger clocking. Information in processor is processed only at single clock edge, for example, positive edge while negative edge is not used to perform useful data processing. We propose to use the following technique (first time in the data center literature): double edge clock triggering where both the positive and negative clock edges are used to process data. The clock frequency, f, can drop to half which will save processor energy significantly due to equation P=$\Sigma\alpha$*C*V2f. The key to implement the above methodology is to employ double edge triggered flip flop (DET FF) that can work on both edges of clock instead of using the conventional single edge triggered flip-flop (SET FF). DET flip-flop have not been reported to be used in any processors in servers in data center so far.

3.1. *Double edge flip flop*

Researchers have proposed different double edge triggered flip-flops, for example, double edge triggered symmetric pulse generator flip-flop (SPGFF) [8], Figure 1 Particularly there was one report about an experiment replacing SET FF by DETFF; project [9] presented a simulation of Leon SPARC CPU (central process unit), synthesized with one of the best commonly used SET FFs—single edge transmission gate master slave flip flop (TGFF) [9], and with SPGFF, using a H-tree with five levels of clock buffers. Characterization for energy and

timing was done on the SPGFF using the trip points in the 0.18um library at the nominal conditions (1.8V, 25°C). The replacement of the SET TGFF with DET SPGFF resulted in clock distribution power savings over 50% and total power saving of processor by 24% [9]. The area of SPGFF is bigger than that of TGFF though. Based on the above result, estimated energy saving of data center will be about 24%*15%= 3.6%, here 15% is the percentage of processor energy in the total energy of data center based on Energy Logic Model.
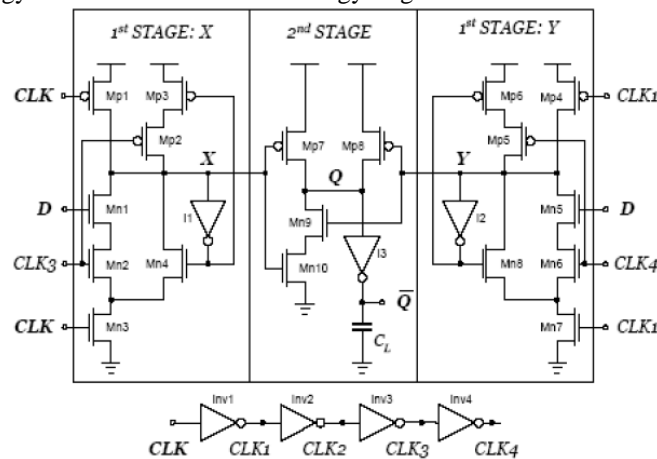

Fig. 1. SPGFF flip flop.

3.2. *Proposed clock branch shared implicit pulsed double edge clock triggered flip flop(CBS_ip)*

However, the previous double edge triggered SPGFF has some power consumption overhead. It has two symmetric stages, it creates a separate internal node on each stage in the critical path. In addition, redundant switching exists in these nodes. These switching consume power but do not produce anything useful; hence, they are redundant switching activities. This increases the overall power consumption of SPGFF since there are four redundant nodes[10]. Toovercome SPGFF's shortcoming and further enhance double edge trigger clocking efficiency, clock branch shared implicit pulsed double edge clock triggered flip flop(CBS_ip)[10] is proposed, Figure 2. Besides dropping clock frequency to half to reduce clock distribution network energy, this flip-flop uses a shared clocked branch which reduces the clocked transistors so local clock load is largely reduced. It improves energy over SPGFF up to 20%. The estimated energy saving of data center will be about 3.6% x 120%=4.3%.

If all the data centers in the world will use double edge clocking CBS_ ip FF in the future, the energy saving will be more than 12 B kWh which is equivalent to more than half month of total energy consumption by Spain, South

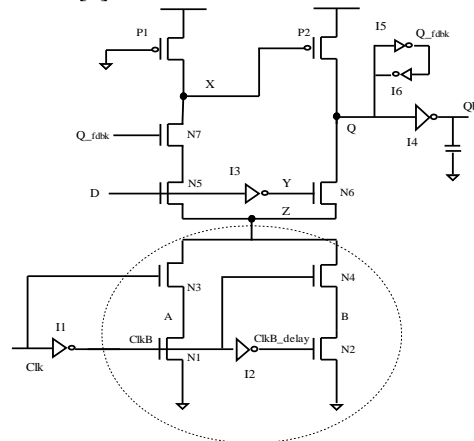Africa, Australia or Taiwan; It will also reduce over 0.7 Million tons of CO based on data from Intel [4].

Fig. 2. Proposed CBS_ip Flip-flop.

4. Conclusion

In this paper, we have illustrated the data center energy usage and its environmental impact. Several low power techniques have been briefly reviewed. A novel low power methodology to save power of processor in data center, double edge triggering technique, is introduced. By using double edge triggering instead of single edge triggering, both clock edges are used and the clock frequency could drop to half, which effectively reduces clock distributing network energy. In addition, using the proposed clock branch shared implicit pulsed double edge clock triggered flip flop , CBS_ip flip-flop, the number of clocked transistors is decreased which further saves the energy. Using CBS_ip flip-flop, the estimated energy saving of the data center could be up to 4.3%, this could lead to a worldwide data center energy saving by 12 B kWh which is equivalent to more than half month of total energy consumption by Spain, South Africa, Australia or Taiwan. It can also reduce 0.7 Million tons of CO based on data from Intel [4]. Hence double edge trigger clocking is a promising way to improve processor energy efficiency in data center to protect environment.

References

1. Gough, Corey, Steiner, Ian, Saunders, Winston (Intel), "*Energy Efficient Servers, Blueprints for Data Center Optimization*", Springer 2015

2. Ren, S., *Power Management in Colocation Data Centers*:
   `http://www.ece.ucr.edu/~sren/project/colo/index.ht`
   `ml`

3. K. Li, "Improving multicore server performance and reducing energy consumption by workload dependent dynamic power management," *IEEE Transactions on Cloud Computing*, in press, 2016.

4. `http://www.intel.com/content/www/us/en/data-`
   `center-efficiency/efficient-datacenter-high-`
   `ambient-temperature-operation-brief.html`

5. `http://www.emersonnetworkpower.com/en-US/Latest-`
   `Thinking/EDC/AboutUs/Pages/default.aspx`

6. Energy Cascade Effect:
   `http://www.emersonnetworkpower.com/en-US/Latest-`
   `Thinking/EDC/Documents/White%20Paper/IS03947_2012_E`
   `nergyLogic_FIN.pdf`

7. `https://www.energystar.gov/products/low_carbon_it_c`
   `ampaign/12_ways_save_energy_data_center/purchasing_`
   `more_energy_efficient_servers_upss_and_pdus`

8. N. Nedović, V. G. Oklobdžija, "Dual-Edge Triggered Storage Elements and Clocking Strategy for Low-Power Systems," *IEEE Transaction on VLSI Systems,* vol..13, Issue 5, pp. 577-590, May 2005.

9. SPGFF synthesis report, `http://www.acsel-lab.com/`
   `Projects/detclocking/documents/motorola_3_12_04.pp`
   `t`

10. P. Zhao, J. McNeely, P. Golconda, "Low Power Clock Branch Sharing Double-Edge Triggered Flip-Flop," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 15, No. 3, pp. 338-345, 2007

11. `http://www.emersonnetworkpower.com/en-US/Latest-`
    `Thinking/EDC/EnergyLogic/Pages/EnergyLogicModel.asp`
    `x`