An ultra-fast miniaturized instantaneous frequency measurement system

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In this paper, an ultra-fast and miniaturized digital instantaneous frequency measurement (DIFM) system is proposed. Based on the high speed clocked comparator and high performance Field Programmable Gate Array (FPGA), the system is constructed. High speed clocked comparator with only 120 ps propagation delay is adopted to replace ADC to do single bit sampling, and FPGA GTH transceivers receive the high speed bits stream. Then the digital processing is done in the FPGA with enjoying shorter processing time comparing with analog IFM. It takes less than 150 ns to output the frequency. Comparing traditional analog with digital method, this design has a smaller area, a higher calculation speed and less power consumption. The design is flexible to reconfigure , easy for operation and it is much more reliable. Our designed IFM receiver has applied to a radar counterwork system.

Keywords: Instantaneous Frequency Measurement (DIFM); High Speed Comparator; FPGA GTH Transceivers; Radar Receiver.

1. Introduction

In modern electronic warfare, the key factor of wining the victory is to make a determination of the characteristic parameters of enemy's radar radiation source quickly and effectively. Among all kinds of characteristic parameters, the signal frequency is one of the important parameters for signals sorting and threats identification, which reflects the radar function. Therefore, the accuracy and instantaneous frequency measurement is particularly important. And, in the actual battlefield environment, there are many kinds of signals with distribution density, high pulse repetition frequency and serious signals overlap [1, 2]. So it is difficult to do signal detection and recognition. It has proposed severe challenges for the function and performance of radar reconnaissance system.

The traditional instantaneous frequency measurement (IFM) systems utilize analog components that may include analog delay line, mixer, power dividers, filters and detectors, transforming the input signal into a video signal. These

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analog components are highly affected by environment temperature and other unexpected factors. So the flexibility, accuracy and consistency are very poor. In recent years, with the development of digital technology, especially in digital signal processor, many digital instantaneous frequency measurement technology has come into being, such as the use of phase estimation method [3], all phase FFT method, but in some situations, they are also very difficult to meet the real-timing requirements. In this paper, the ultra-high speed comparator and Field Programmable Gate Array (FPGA) are adopted to construct the IFM system. High speed clocked comparator with only 120 ps propagation delay is adopted to replace ADC to do single bit sampling, and FPGA GTH transceiver receive the high speed bits stream. Then the digital processing is done in the FPGA with enjoying shorter processing time comparing to analog IFM. Our designed IFM receiver has applied to a radar counterwork system.

This article is organized as follows: Section II introduces the principle of digital instantaneous frequency measurement. The design of system structure is described in detail in section III. Section IV describes data processing of auto-correlation. At last, the article is concluded in section V.

2. The Principle of Digital Instantaneous Frequency Measurement

The auto-correlation operation can be very convenient to extract the characteristic information of the signal in time domain. Assuming a single carrier frequency signal,

$$s(t) = \cos(2\pi f_c t + \varphi) \tag{1}$$

Where, f_c is the carrier frequency, φ is the initial phase of signal. In the analysis, we assume that the phase is not change with time. A period of τ time is delayed, $s(t)$ becomes into the following equation,

$$s(t-\tau) = \cos\left(2\pi f_c (t-\tau) + \varphi\right) \tag{2}$$

Eq. (1) and Eq. (2) make a correction operation and low pass filtering, we get Eq. (3),

$$y(\tau) = \cos\left(2\pi f_c \tau\right) \tag{3}$$

From Eq. (3) we can know that the results of auto-correction has nothing to do with time t, but only relate to the time delay. When known the time delay, and the correction calculation results, we can calculate the signal frequency value. At the same time, due to the cosine function is periodic, the frequency

value derived from the Eq. (3) is ambiguous. In order to obtain the unambiguous frequency value, the time delay value τ must has a limit, that is, when time delay $\tau < 1/2 f_c$, the frequency is unambiguous.

Digital sequence is obtained after the input analog signal is sampled. Before doing the correlation operation, the bits shift operation should be done. The signal frequency can be calculated according to the correlation results. The number of digital sequence shifted bits represents the time delay of analog signal. For an incoming bit streams b_k , consisting of N bits, the auto-correlation for a delay of d bits is defined as Eq. (4),

$$C_d = \sum_{k=0}^{N-1} b_k b_{k-d} \tag{4}$$

The results have only N discrete values and may not provide the desired accuracy and resolution. Increasing the delay d improves the situation. However, increasing the delay d would cause frequency ambiguous. Fig. 1 shows the relationship between delay d and auto-correlation results. In the design, N is 256, d_1, d_2, d_4, d_6 represent one bit shift, two bits shift, four bits shift and six bits shift. As we can see, result of one bit delay will only provide a very rough frequency estimation. Therefore, we have picked a group of specified delay d to get an accurate frequency [4, 5].

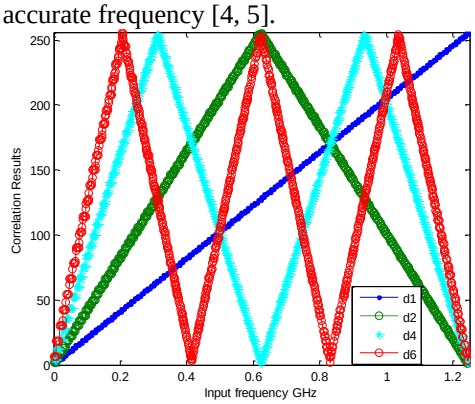

Fig. 1 The relationship between delay d and auto-correlation results

3. Design of System Structure

The system structure is mainly composed of a high speed comparator and a high performance FPGA. The high speed comparator mainly replaces ADC to do single bit sampling, and data processing and frequency calculation is completed by FPGA. The IF or RF single-ended signal that comes from RF circuit board is converted into differential signal through a balun. Then the differential signal is

sent to the high speed comparator. Under the drive of clock, the comparator completes single bit sampling. The comparator generates '1' when the logic level of the non-inverting input terminal is greater than inverting input, and generates logic '0' when the non-inverting input smaller than the inverting input. The driving clock also comes from the RF circuit board and is divided into two pairs of differential signal by a clock buffer. One pair of different clock signal is sent to the comparator, and another one is sent to FPGA. The FPGA GTH transceiver reference clock is produced by dividing the input buffer clock. Therefore, the clock signals used on the processing procedure is phase coherent.

The main hardware structure of the system is shown in Fig. 2. It mainly consists of a high speed comparator HMC874LC3C produced by Analog Device corporation and Xilinx 7 series FPGA XC7VX690T. The HMC874LC3C is an ultrafast comparator. The comparator supports 20 Gbps operation while providing 120 ps clock to data output delay. Also, it only has 150 mW power consumption [6]. The input bandwidth can be up to 10 GHz and it can meet many requirements of bandwidth signal. At the same time, it has a very small area and can save the area of the circuit board, thus saving the cost.

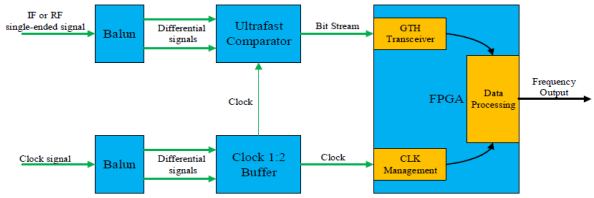

Fig. 2 The main hardware structure of the system

Xilinx 7 series FPGA is the representative production of high-performance digital processors. It adopts 28 nm production technics, the real 6 input look-up table and owns greater internal memorizer and high speed signal processing capability. The clock management module and phase locked loop module can generate many precise frequency clock signals. In terms of peripherals, it also has a large number of ordinary IO ports as well as the high speed serial transceivers, and its transmission speed can reach about 28 Gbps. In our design, we adopts XC7VX690T FPGA. Its GTH transceiver speed can reach about 13.1 Gbps and its performance can meet the requirements of the output data rate of high-speed comparator. At the same time, the FPGA has less power consumption, more signal processing module and can reach the real-timing processing demands.

The 7 series FPGA GTH transceivers are power-efficient transceivers, supporting line rates from 500Mb/s to 13.1Gb/s [7]. The GTH transceiver is

highly configurable and integrated with the programmable logic resources of the FPGA. The transceiver can support a wide variety of applications, especially in high speed design situation, such as Serial RapidIO, PCI Express, Giga-Byte Ethernet and other board to board high speed serial data transfer. There are 80 GTH transceivers in XC7VX690T FPGA, each transceivers consists of Transmitter, Receiver and some shared resources. In the design, the receiver function is only used, so the transceiver is disabled.

Each GTH transceiver includes an independent receiver, made up of a PCS and a PMA. High-speed serial data flows from traces on the board into PMA of the GTH transceiver RX, into the PCS, and finally into the FPGA logic. The bit stream is pre-processed by the PMA and PCS module, and then flows to FPGA logic module for following procedure.

4. Data Processing of Auto-correlation

In our design, 10 GHz as the clock of comparator is chosen. So the rate of bit stream is 10 Gbps. We need to reduce the data rate for the purpose of processing conveniently. The serial data should be transformed into parallel data. If the parallel data width is 40 bits, the rate decreases to 250 MHz. The high speed serial bit stream is divided into several 40 bits stream. So the auto-correlation operation can be done in each 40 bits stream. Then calculates the result. If we only use one group 40 bits data to calculate the signal frequency, the frequency measurement error will be large. Therefore, we adopts several group 40 bits data for pipeline operation. We define the pipeline stage is 20, and the 800 bits data flow will obtained. After 20 groups is done, using all the results to calculate the signal frequency.

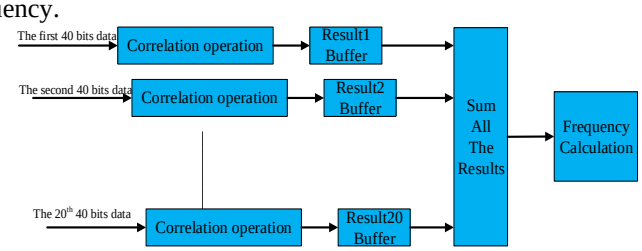

Fig. 3 The diagram of pipeline for calculating the frequency

Fig. 3 shows the diagram of pipeline for calculating the frequency. Each 40 bits data calculate the result of auto-correlation. The 20 groups of 40 bits data calculate the frequencies simultaneously and the results flow into a buffer. At last, the last stage calculates and outputs the frequency. Comparing to the traditional using analog devices, the digital design method is flexible to adjust

and more accuracy. Meanwhile, the digital IFM devices rely less on environmental conditionals.

5. Conclusion

In this paper, an ultra-fast and miniaturized digital instantaneous frequency measurement system is proposed. With the help of high speed comparator and Xilinx high performance 7 series FPGA, we can calculate the signal frequency in real time. This digital instantaneous frequency measurement architecture is very flexible, reliable and practical. The ultra-fast frequency measurement, the less measurement error, and the highly configurable structure, making the system suitable for many radar systems. The design of the comparator and GTH transceiver architecture is very effective in the digital receiver. This design has proven to own good performance, practicality as well as large economic value.

Acknowledgments

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