Study on Time Synchronization of Marine Fault Recording Device Based on Lagrange Once Interpolation Algorithm

Leiming Huang[1, a], Liming Wang[2,b], Zhongqin Chen[3,c]
[1,2]College of Electrical Engineering, Naval University of Engineering, China
[3]College of Computer Science, South Central University for Nationality, China
[a]18674086511@163.com, [b]13006305743@163.com, [c]1242513816@qq.com

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Abstract. The external clock synchronization method is difficult to implement, susceptible to interference and insecure for the marine fault recording device, so a synchronous method based on Lagrange once interpolation algorithm is proposed. MATLAB simulation and prototype test show that the synchronization accuracy can meet the T4 level specified in IEC61850 standard, and the error has no impact on the later fault analysis.

Introduction

The fault recording device is a kind of intelligent equipment commonly used in the national grid, which can record the transient process before and after the fault, thus providing the original reference for locating fault line quickly and judging the cause of the fault accurately, and is gradually applied in the marine power monitoring field. Because most of the parameters of marine power system change with time, discrete data of different sampling channels such as current and voltage can only be brought into the analysis algorithm after corresponding to the same time, which involves the problem of time synchronization. Although the development of external clock synchronization method is very mature, it is not applicable to the complicated working environment of ship power system. This paper aims to introduce Lagrange once interpolation algorithm into the data synchronization to improve the maritime adaptation ability of the fault recording device.

Limitations Analysis of the External Clock Synchronization Method

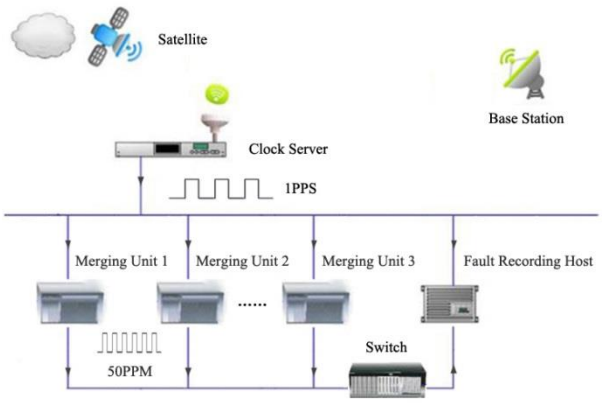

Fig. 1 Time Synchronization of Fault Recording Based on External Clock

At present, the external clock synchronization method is commonly used in the terrestrial fault recording device, which relies on an external clock source to achieve time uniform[1], as shown in Fig. 1. By configuring the timing signal receiver for the power station and taking it as master clock， the intelligent devices obtain accurate second pulse signal and UTC from the clock server[2]. The merging unit calibrates its own internal clock to synchronize with the master clock, then uses the multiplier function of the internal crystal to control the electronic transformers for high frequency synchronous sampling. Each merging unit sends the message data including sampling time to the fault recording

host through the switch at an unified time interval, and the host decides whether to start the recording function according to the internal setting condition.

Although this method ensures that time information is consistent at the source, there still exist the following deficiencies in terms of feasibility, reliability, security, etc.

(1) At present, the satellite signal receiving system installed on the ship is mainly for the navigation and positioning services. Even if the clock server is added, it is also very troublesome for the fault recording device in the bilge distribution cabinet to access the main clock signal from the upper deck.

(2) The ocean climate condition is relatively poor, furthermore the ship power environment is complicated, so the satellite synchronization signal based on wireless transmission is easy to be lost or disturbed, resulting in the entire system time information disorder.

(3) As the external clock signal needs to be processed by the receiver, and then released by the clock server, it will lead to the entire synchronization network paralysis once the receiver or clock server fails. What's more, the fault recording device needs to be configured with an additional clock input interface[3] and high-precision punctual crystal, which increases the design difficulty and cost.

(4) Synchronization signal is generally taken from the satellite system, in which GPS is controlled by the U.S. Department of Defense[4], not meeting the national security development strategy, and Chinese BDS is not yet mature, which is limited to serving the Asia-Pacific region currently[5].

As the external clock synchronization method overly depends on the stability of the clock source, it does not apply to the complex working environment of the ship power system. Therefore, the interpolation algorithm is introduced into the data synchronization of marine fault recording device, and the precision of Lagrange once interpolation is verified by simulation analysis and prototype test.

Realization of Interpolation Synchronization for Fault Recording Data

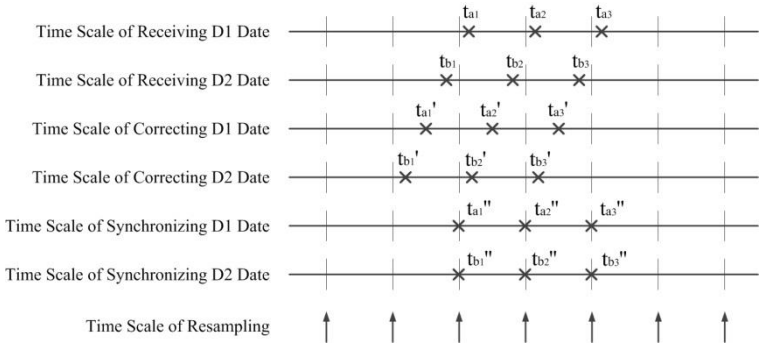

Fig. 2 Resampling Process of Interpolation Synchronization

The realization of interpolation synchronization for marine fault recording device is shown in Fig. 2: After receiving the packets from the merging units DU1 and DU2, the host extracts the serial number, the sampling value, the delay time and other information, and restores the actual sampling time t_{an}' and t_{bn}' after the receiving time t_{an} and t_{bn} subtract the rated delay Δt. Then, the internal clock of the host generates a resampling pulse signal, and a synchronous value at t_{an}'' and t_{bn}'' can be obtained by interpolation algorithm. The sampling points are continuously moved backwardly, and finally a new sequence is obtained.

There are many interpolation algorithms, including Newton interpolation, Hermite interpolation, the least squares method, etc. As Hermite interpolation satisfies that both valuation and derivative are equal to the real value, it has been applied widely. However, as the sampling points can reach tens of hundreds and the frequency is usually several kilohertz, if using Hermite interpolation, FPGA and CPU need to deal with massive data, which will directly affect real-time response and stable operation of the fault recording device. This thesis mainly studies Lagrange interpolation algorithm, which is based on the consideration of the accuracy, the amount of calculation and the difficulty of realization.

Simulation Analysis of Lagrange Once Interpolation Synchronization

Lagrange interpolation formula and the remainder equation are

$$L_n(x)=\sum_{k=0}^{n}[\prod_{\substack{j=0\\ j\neq k}}^{n}\frac{x-x_j}{x_k-x_j}]\,y_k \qquad R_n(x)=\frac{f^{(n+1)}(\xi)}{(n+1)!}\omega_{n+1}(x) \tag{1}$$

It can be seen from Eq. 1 that Lagrange interpolation is related to the number of original sampling points involved in the operation[6], and the following takes the current function $i(t)$ as an example to analyze Lagrange interpolation. Suppose that the host receives two packets sent by the same merging unit and obtains two discrete points $[t_k,i(t_k)]$ and $[t_{k+1},i(t_{k+1})]$. The current value at the synchronization time t can be obtained by Lagrange once interpolation algorithm

$$L_1(t)=\frac{t-t_{k+1}}{t_k-t_{k+1}}i(t_k)+\frac{t-t_k}{t_{k+1}-t_k}i(t_{k+1}) \tag{2}$$

As an approximation of the actual value $i(t)$, the error caused by Lagrange once interpolation is

$$R(t)=\left|i(t)-L_1(t)\right|=\left|\frac{1}{2}i''(\xi)(t-t_k)(t-t_{k+1})\right| \tag{3}$$

In Eq. 3, $i''(\xi)$ is the second derivative of $i(t)$, ξ is a moment in the interval $[t_k, t_{k+1}]$.

In order to further verify the synchronization accuracy of Lagrange once interpolation algorithm, the simulation analysis is carried out by MATLAB. Assuming that the sampling frequency of the merging unit is 1000Hz, which means that there are 20 sampling points per cycle under f=50Hz, and the input signal contains DC, fundamental wave and third harmonic

$$i(t)=0.3+5\cos(2\pi ft)+1.7\cos(6\pi ft+\pi/30) \tag{4}$$

After receiving the packets from the different merging units, the host resamples at 1000Hz, and the time difference between the synchronization point and the reference point is t-t_k=2μs. According to Lagrange once interpolation algorithm and the simulation results of a cycle is shown in Fig. 3.

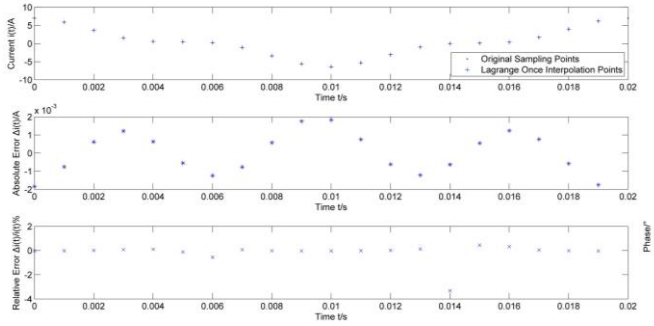

Fig. 3 Error Analysis

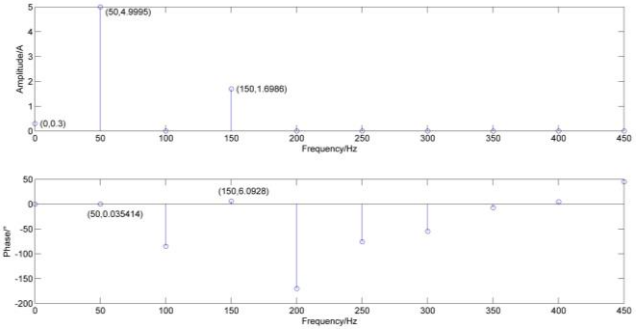

Fig. 4 FFT Analysis

It can be seen that the absolute error varies with the waveform curvature between two adjacent original sampling points. The better the range of linearity is, the smaller the absolute error is. Since the linearity of the fundamental wave is greatly influenced by the harmonic components, the absolute error increases when the third harmonic reaches the position of crest and valley. In addition to the individual points, the relative error is basically less than 0.45%. Table 1 lists the maximum of absolute error and relative error among one-cycle caused by Lagrange once interpolation.

Table 1 Maximum Error Analysis of Lagrange Once Interpolation Simulation

	t [s]	$i(t)$ [A]	$L_1(t)$ [A]	$\Delta i(t)$ [A]	$\Delta i(t)/i(t)$ [%]
Maximum of Absolute Error	0.010002	-6.390348	-6.388516	0.001832	-0.0287
Maximum of Relative Error	0.014002	0.019103	0.018469	0.000634	3.3189

The fft (X, n) function of MATLAB can perform the amplitude and phase analysis of the 20 synchronization points, as shown in Fig. 4. It can be seen that the amplitude error is very small compared with the original sampling signal at 0Hz, 50Hz and 150Hz. The relative error shown in Table 2 is less than 0.1%, which is almost negligible. The phase error of the fundamental wave and third harmonics is no more than 0.040 °and 0.100 °respectively, and the equivalent time delay is

$$\varepsilon_1 = \frac{0.035414 - 0}{360 \times 50}\text{s} = 1.967\mu\text{s} \qquad \varepsilon_3 = \frac{6.0928 - 6}{360 \times 150}\text{s} = 1.719\mu\text{s} \tag{5}$$

Both are not more than 2μs, meeting the T4 level of IEC61850 standard (± 4μs).

Prototype Test of Lagrange Once Interpolation Synchronization

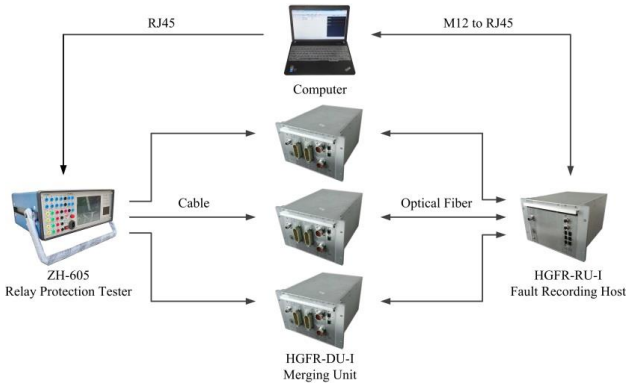

Fig. 5 Test Platform

	THD	RMS	DC	1	5
V L1-N	10.103%	57.700V	0.000V	57.408V	5.800V
				0.000°	0.000°
V L2-N	10.103%	57.700V	0.000V	57.408V	5.800V
				240.000	240.000
V L3-N	10.103%	57.700V	0.000V	57.408V	5.800V
				120.000	120.000

Fig. 6 Add the Fifth Harmonic Voltage

Combined with the characteristics of ship power system, this thesis has designed a set of marine fault recording prototype named of HGFR-I, and its synchronization performance has been veried through the test platform, as shown in Fig. 5.Firstly, the relay protection tester outputs three-phase AC voltage signals to three merging units, of which the valid value is 57.7V, frequency is 50Hz, and phase angle difference is 120 °. Secondly, the sampling frequency of prototype is set to 4000Hz, and the limit value of the fifth harmonic proportion in the three AC voltage channels is modified to 10.0%. Lastly, the relay protection tester adds the fifth harmonic proportion to 10.103%, as shown in Fig. 6.

Table 2 RMS Error Analysis under Fault Condition

Fundamental RMS / Group		Original Value[V]	Measured Value[V]	Absolute Error[V]	Relative Error[%]
T1	Ua	57.408	57.405	-0.003	-0.005
	Ub	57.408	57.410	0.002	0.003
	Uc	57.408	57.411	0.003	0.005
T2	Ua	57.408	57.406	-0.002	-0.003
	Ub	57.408	57.410	0.002	0.003
	Uc	57.408	57.410	0.002	0.003
5^{th} Harmonic RMS / Group		Original Value[V]	Measured Value[V]	Absolute Error[V]	Relative Error[%]
T1	Ua	5.800	5.776	-0.024	-0.414
	Ub	5.800	5.776	-0.024	-0.414
	Uc	5.800	5.775	-0.025	-0.431
T2	Ua	5.800	5.776	-0.024	-0.414
	Ub	5.800	5.777	-0.023	-0.397
	Uc	5.800	5.776	-0.024	-0.414

Table 2 lists the RMS error of the three-phase AC voltage at any two time points:

(1)The observed values of the fundamental wave almost fall around 57.410V, and the maximum of absolute error and relative error do not exceed ± 0.004V and $\pm 0.006\%$ compared with the original value 57.408V, and the precision satisfies the fault analysis requirement.

(2) The measured error of the fifth harmonic is slightly larger, which is basically maintained at -0.024V. The error is caused by three main reasons: First, the output accuracy of the fifth harmonic is lower; Second, the curvature of the fifth harmonic changes more unstably; Third, in the process of extracting the harmonic components, Fourier algorithm will bring a larger calculation error[7].

Table 3 Phase Errors Analysis under Fault Condition

Fundamental Phase / Group		Measured Value[°]	Original Phase Difference[°]	Measured Phase Difference[°]	Absolute Error[°]	Relative Error[%]	Equivalent Time Delay[μs]
T1	Ua	-24.985	0	0	0	0	0
	Ub	-145.020	-120	-120.035	-0.035	0.029	-1.944
	Uc	94.961	120	119.946	-0.054	-0.045	-3.000
T2	Ua	128.036	0	0	0	0	0
	Ub	8.009	-120	-120.027	-0.027	0.023	-1.500
	Uc	-112.008	120	119.956	-0.044	-0.037	-2.444
5th Harmonic Phase / Group		Measured Value[°]	Original Phase Difference[°]	Measured Phase Difference[°]	Absolute Error[°]	Relative Error[%]	Equivalent Time Delay[μs]
T1	Ua	-125.401	0	0	0	0	0
	Ub	114.424	-120	-120.175	-0.175	0.146	-1.944
	Uc	-5.511	120	119.890	-0.110	-0.092	-1.222
T2	Ua	-80.234	0	0	0	0	0
	Ub	159.582	-120	-120.184	-0.184	0.153	-2.044
	Uc	39.631	120	119.865	-0.135	-0.113	-1.256

As shown in Table 3, regarding A-phase as the benchmark, the absolute error of fundamental phase and the fifth harmonic phase does not exceed -0.060 °and -0.200 °respectively, and the equivalent time delay is maintained below -3.5μs, conforming to T4 level of IEC61850 standard.

Conclusions

The external clock synchronization has many limitations for the marine fault recording device. This thesis has designed a synchronization method based on Lagrange once interpolation algorithm, which is verified through MATLAB simulation and the prototype test. The results show that the RMS error is almost negligible, and the equivalent time delay corresponding to the phase error can be controlled within ±4μs demanded by IEC61850 standard.

References

[1] Kun Liu, Youqing Zhou, Wuyang Zhang and Guiqing Wu: submitted to Telecommunications for Electric Power System (2006) In Chinese
[2] Huangsheng Hua, Li Wang: submitted to Telecommunications for Electric Power System (2011) In Chinese
[3] Yanjun Fang, Fengfei Yi, Ruimin Chen and Zhengmin Kong: submitted to Automation & Instrumentation (2013) In Chinese
[4] T. Matsuyama, K. Abe, R. Kashiwa and T. Takada: submitted to Research Memoirs of the Kobe Technical College (2001)
[5] F.G. Toro, U. Becker and D.E.D. Fuentes: submitted to IFAC-ParersOnLine (2016)
[6] T. Sauer and Yuan Xu: submitted to Mathematics of Computation (1995)
[7] F.J. Harris: submitted to Proceedings of the IEEE (1978)