Isolated Streetlight LED Driver Design

HUANG Jian
XiJing University, Xi'an 710123, China
565200245@qq.com

Keywords: LED Driver；Power Factor; THD

Abstract. LED lighting is being used for residential, commercial and industrial applications. It offers various advantages over incandescent bulbs, such as lower energy consumption, longer life, attainment of full brightness without need for a warmup time, and so forth. With the advent of these lights in large numbers, regulations in a few countries require LED drivers with high power factor (greater than 0.9) and low current THD (less than 10 per cent), to have minimum effect on the grid.

1 Principle of Operation

The UCC28810 is an off-line AC/DC controller specifically designed to drive high power LEDs for lighting applications requiring power factor correction and EMC compliance. It is designed for controlling a Flyback, single-ended primary-inductance converter (SEPIC), or Boost converter operating in critical conduction mode. The UCC28810 features a transconductance amplifier for feedback error processing, a simple current reference generator for generating a current command proportional to the input voltage, a current-sense (PWM) comparator, PWM logic, and a totem-pole driver for driving an external FET. To overcome the issue of high ITHD, these subsystems internal to low-cost UCC28810 are used here to operate at fixed switching frequency with constant on-time, and achieve high power factor and low ITHD, less than 10 percent.

Figure 1 depicts a reference schematic describing key components in the Flyback stage. Input AC voltage is rectified using full bridge rectifier (D1A–D4A) to obtain a unidirectional AC bus. It may be noted that the input capacitor is so small (220nF) that the input voltage is close to a rectified sinusoid, as also required to obtain high power factor. This rectified VIN is connected through transformer primary winding to the drain of switching FET Q3, whose source is connected to ground return through the current-sensing resistor R24.

The transformer primary inductance, Lp is related to the switching frequency fsw, converter output power Pout, system efficiency η, maximum on-time, ton-max at minimum input line voltage Vin(min)according to the equation 1.

$$L_p = \frac{\eta \times V_{in}^2 \times t_{on-max}^2}{2P_{out} \times \frac{1}{f_{sw}}} \tag{1}$$

Primary inductance, Lp is chosen as 200 μH for this design. Maximum on-time at minimum input voltage is chosen as 7.5 μsec, considering maximum duty cycle of 45% at 60 k Hz switching frequency. According to the equation 2.

$$I_p = \frac{V_{in} \times t_{on-max}}{L_p} \tag{2}$$

1.1 Active Startup Circuit

Figure 1 illustrates the active startup circuit.

It is not possible to supply bias voltage while meeting IC current requirements for both UCC28810 and CD74HCT14 together using the resistive startup technique. In Figure 1, transistor Q8 as emitter-follower sources 17.4 V VDD startup bias for UCC28810 at its emitter, which is converted to 5V for CD74HCT14 supply using discrete, low-IQ linear regulator. Once switching begins and output voltage ramps-up, bias voltage for these ICs is sourced from primary-side

auxiliary winding, which is also used to disable active-startup circuit with Q6. Once in steady state, it is required to disable active-startup circuit in order to minimize efficiency loss due to large voltage drop across Q8 and IC supply current flowing through it.

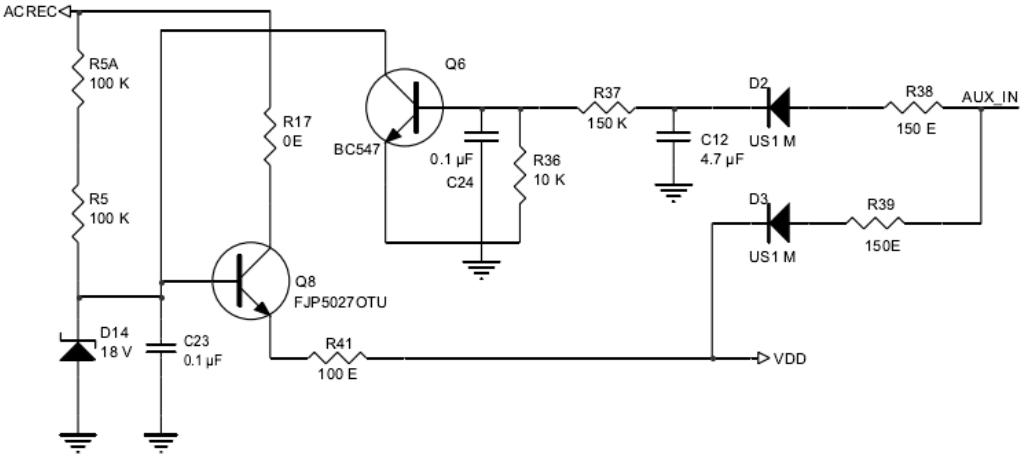

Fig 1. Active Startup Circuit

1.2 Switching Oscillator

Figure 2 shows the switching oscillator circuit.

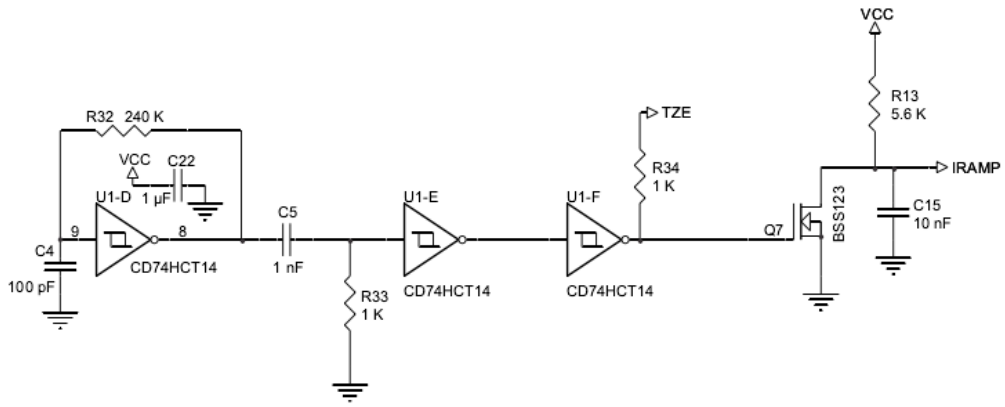

Fig 2. Switching Oscillator

The flyback stage is operating at a constant 60-k Hz switching frequency, generated using CD74HCT14, Schmitt-triggered inverter, as shown in Figure 2. Equation 3 is used to calculate oscillator frequency of a Schmitt inverter-based oscillator. For C4= 100 p F, feedback resistance R32 is obtained as 248 kΩ:

$$f_{sw} = \frac{1}{0.67RC} \tag{3}$$

1.3 Soft-Start Circuit

At startup, the 60-k Hz switching begins as soon as bias on UCC28810 exceeds its VDD turn-on threshold(15.8 V). Due to the use of the 470-n F capacitor C20 to slow down loop response, it is required to have soft-start operation, such that the duty cycle increases gradually from its minimum value at startup. The circuit in Figure 3 shows this implementation. As VCC bias voltage (5 V) is formed during startup, RC low-pass filter (R10= 2.2 M, C11= 4.7 µF) charges slowly to input peak value, resulting in Q1 pulling down error amplifier output (EAOUT) low, initially, and allowing it to reach its final value after approximately a 1- second delay. Diode D6 helps to discharge C11 for next soft-start initiation on VDD/ system reset.

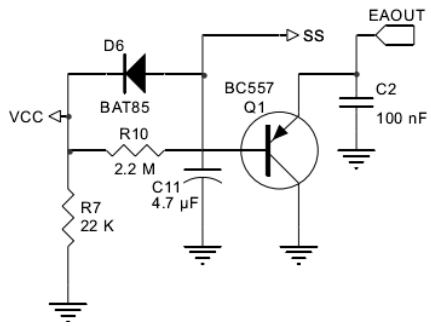

Fig 3. Soft-Start Circuit

Additionally, duty cycle limiting at nearly 45% is incorporated to mitigate stability issues, by providing DC voltage on the VINS pin as UCC28810 internal multiplier output clamp. For 60-k Hz switching frequency, the feedback ramp on C15 reaches a level of 0.53 V at 45% duty cycle. Since UCC28810's internal multiplier has a fixed gain of 2, an input of 0.26 V DC on the VINS pin helps clamp the duty cycle at maximum 45%.

1.4 Output Current Regulation

We need to regulate constant 600-m A output current though the LEDs. This is achieved using both secondary-side and primary-side regulation circuits. With secondary-side output current regulation, current through the LEDs is measured as a voltage on very small current sense resistors (R29 and R31), and regulated with TL431's 2.495 V feedback reference. This circuit is shown in Figure 1. VDD voltage for the optocoupler and TL431s is generated with a 12-V zener biased from the 106-V output voltage. During the process of locking of loop to reach regulation, when the voltage on U4 REF pin exceeds 2.495 V, the cathode of U4 pulls down optocoupler U3 cathode to 2.495 V, which reduces voltage on the EAOUT pin of UCC28810. Since EAOUT pin of UCC28810 is output of internal error amplifier, this pulldown with optocoupler helps to maintain duty cycle optimum for output current regulation point. Further, power loss on sense resistors is proportional to voltage across them and the current flowing through them:

$$P_{loss} = V_{sense} \times I_{LED} \tag{4}$$

2 Test Results

2.1 Secondary-Side Output Current Regulation

Table 1 lists the performance characteristics of a 70-W LED driver design with secondary-side output current regulation.

Table 1. Performance Characteristics of 70-W LED Driver Design With Secondary-Side Output Current Regulation

Input RMS Voltage (V)	Input Power (W)	Output Voltage (V)	Output Current (mA)	Output Power (W)	Efficiency (%)	Power Factor	Current THD (%)
90	71.35	105.8	586	61.99	86.89	0.996	4.67
120	69.55	106	587	62.22	89.46	0.997	3.25
150	68.85	106.1	586	62.17	90.30	0.998	2.67
180	68.68	106.1	586	62.17	90.52	0.998	2.56
220	67.91	106.1	586	62.17	91.55	0.998	2.54
250	68.12	106.2	586	62.23	91.35	0.999	2.55
265	68.17	106.2	586	62.23	91.29	0.998	2.97

2.2 Primary-Side Output Current Regulation

Table 2 lists the performance characteristics of a 70-W LED driver design with primary-side output current regulation.

Table 2. Performance Characteristics of 70-W LED Driver Design with Primary-Side Output Current Regulation

Input RMS Voltage (V)	Input Power (W)	Output Voltage (V)	Output Current (mA)	Output Power (W)	Efficiency (%)	Power Factor	Current THD (%)
90	79.41	112.6	621	69.92	88.05	0.999	3.88
120	78.25	112.3	622	69.85	89.26	0.999	3.58
150	75.3	111.0	611	67.82	90.06	0.999	2.12
180	73.57	109.9	605	66.48	90.37	0.999	1.92
220	69.37	107.5	595	63.96	92.20	0.998	2.80
250	70.69	108.3	599	64.87	91.77	0.998	2.26
265	70.93	108.4	598	64.82	91.39	0.997	2.25

3 Conclusion

This application report describes design details and test results for a fixed-frequency, single-stage 70-WAC/DC flyback LED driver for streetlight applications, both with primary-side and secondary-side output current regulation circuits. Due to constant on-time and fixed switching-frequency operation, power factor greater than 0.9, and current THD less than 10 percent, is easily achieved. This design meets all the necessary performance specifications, including output open-circuit and short-circuit protections.

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