Design of infrared imaging processing system for uncooled LWIR base on UAV platform

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Abstract. For uncooled LWIR system function limitations and lack of real-time image processing problems. The design scheme of high performance uncooled LWIR image processing system based on UAV system platform is proposed. The solution uses TI's TMS320C6657 DSP and Altera's EP3C25F324 FPGA processor as the system computing core, makes the long wave infrared image acquisition, FPGA image preprocessing, DSP image processing into one. And designed a set of systems in line with the external needs of the communication program.

Introduction

With the continuous development of infrared image processing technology, with the small size, low power consumption, processing performance and other advantages are widely used in domestic and foreign military fields, civil areas and commercial areas[1]. Face UAV system platform, currently on the market of uncooled long wave infrared imaging processing system is limited. Because of its focus on the completion of infrared detector imaging, while ignoring the complex image real-time processing, such as target recognition, target tracking and other functions. For the problem, based on the TMS320C6657 DSP and EP3C25F324 FPGA processor, this paper designs a set of complex systems with uncooled LWIR imaging and processing functions[2]. The system not only to achieve the acquisition of infrared images, complete the conventional infrared image algorithm, but also according to the actual mission requirements, complete complex image tracking, matching algorithms, as well as infrared camera control, infrared image preprocessing, image complex algorithm work. That is suitable for UAV platform needs, and post-system requirements to provide sufficient space to upgrade[3].

System Overview

The system architecture is shown in Fig.1.The overall structure of the system uses four board stack serial connection. Respectively, LWIR detector board, FPGA image preprocessing board, DSP image board and power interface board.

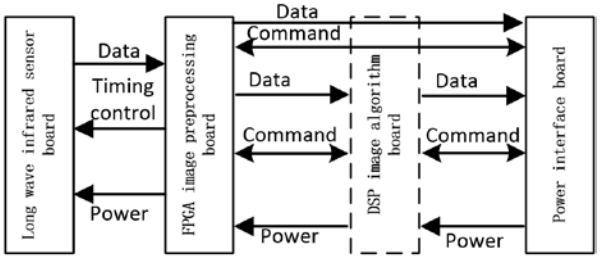

Fig.1.System architecture

LWIR detector cell design

LWIR detector cell is mainly integrated with long-wave infrared detector-related bias voltage, power supply, ADC data conversion, temperature control circuit. This part is the key to imager imaging.

LWIR detector characteristics. The system selects ULIS UL04371-042 detector[4], its features include high sensitivity, small size, light weight, low supply voltage. It is suitable for non-refrigerated thermal sensing imaging system, as shown in Fig.2.

Fig.2.ULIS uncooled LWIR detector

The detailed parameters of the UL04371-042 detector are shown in Table 1. One of the more important parameters is the physical matrix pixel and noise equivalent temperature difference, Physical matrix pixels directly affect the image size after imaging. The noise equivalent temperature difference affects the quality of the image after the effect.

Table1 UL04371-042 parameters

parameter name	Parameter value
Physical matrix pixels	640×480
Pixel spacing	25μm
Noise equivalent temperature difference	60mK≤NETD≤80mK @f/1,300K,50Hz
Power consumption (not including TEC)	≤300mW
Sensitive area size	16 mm ×12 mm
Detector size	23.5 mm ×32 mm ×7.7 mm
Weight	≤25g

LWIR detector unit scheme. The system can select two frame rate outputs, if you select the 25Hz frame rate, the single analog output. If you select 50Hz frame rate, you need to use dual analog output. The dual analog output is converted to 14-bit parallel data by the AD9240. To save FPGA resources, using the serializer to convert the multiplexed data to 4 pairs of LVDS to the FPGA image preprocessing unit. As the detector built-in temperature sensor, using ADN8830 feedback circuit to achieve the detector temperature control function [5]. The design of LWIR detector board program is shown in Fig.3.

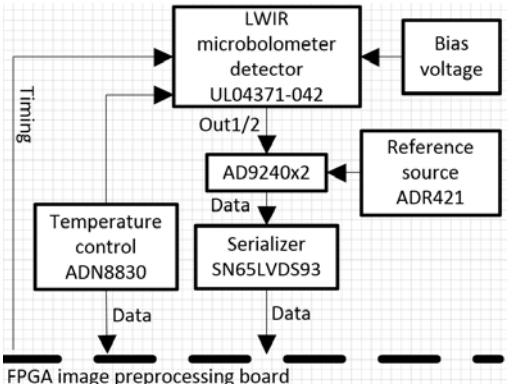

Fig.3. LWIR detector board diagram

FPGA image preprocessing and DSP image algorithm unit design

FPGA preprocessing unit design. The system FPGA image preprocessing unit core processor selected Altera Corporation Cyclone III series EP3C25F324. The processor has low power consumption, low cost, and mature technology and can be quickly applied to the system design. FPGA image preprocessing unit function is divided into three parts, including communication with long-wave infrared detector unit, DSP image algorithm unit communication and power interface unit communication, as shown in Fig.4.

LWIR detector unit communication includes timing control for long-wave infrared detectors and receiving the long-wave infrared detector output image data. After the image data is preprocessed, it is transmitted to the DSP image algorithm unit through two UPP interfaces. Single highest data transfer rate of up to 150MB / s. In addition, with the DSP image algorithm unit communication interface also includes a UART and a SPI, used to achieve instruction communication. The power interface unit communication includes multiple LVDS signals and one UART interface, the LVDS signal is used to directly output the image data pre-processed by the FPGA, and the UART interface is used for communication between devices outside the imager. The main work of the unit is to sort the image data and simple image preprocessing algorithm to reduce the pressure of the DSP image algorithm unit.

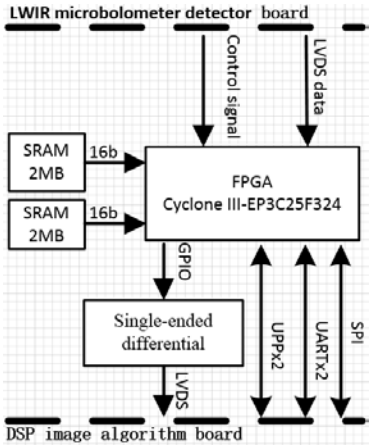

Fig.4.FPGA image preprocessing board diagram

DSP image processing unit program design. The unit uses TI's TMS320C6657 DSP as the core processor, there are two C66x cores in DSP. Each kernel frequency up to 1.25GHz and supports a variety of high-speed standard interface. Including Rapid Release 2, PCI Express Gen2 and Gigabit Ethernet[6].According to DSP image algorithm unit function requirements, the program is shown in Fig.5. With FPGA image preprocessing unit communication using SRIO, SPI, UART, UPP interface, SRIO interface with 2x 2.1 version, compatible with future higher performance FPGA. SPI and UART interfaces are used as command communication interfaces during processing. UPP interface with dual-channel design, each channel data line width up to 16bit, synchronous clock rate up to 75MHz. This interface can meet the image data transmission rate requirements, the remaining data transmission capacity to be compatible with a larger amount of data system. Communication with the power interface unit using SGMII, UART interface. SGMII interface which using Gigabit Ethernet standard design, the rate reached 1.25Gbps. The DSP-processed image data is uploaded to the PC by the power interface unit Ethernet. The UART interface uses two-wire mode, outputs to the power interface unit and communicates with the imager's external device. In addition, to meet the computing needs of the algorithm, DSP is equipped with two DDR3 memory chips. The total capacity of 1GB, the data is wide for the 32bit, the clock rate of 667MHz. For the storage of a large number of image data, equipped with a DSP for the NAND Flash which capacity is 1GB. DSP boot mode is used I2C interface EEPROM chip which capacity is 1MB.

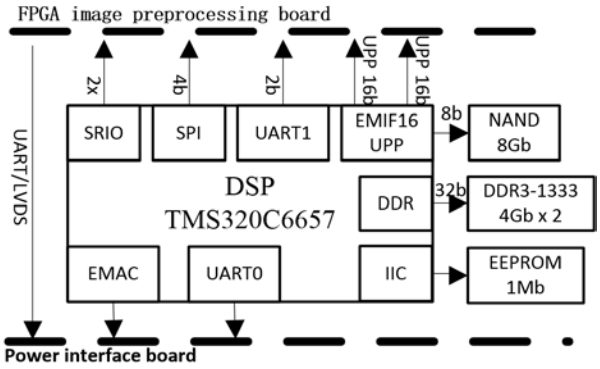

Fig.5.DSP image processing algorithm board diagram

High-speed UPP interface logic design

To ensure that the system image processing real-time high, the system image transmission using UPP high-speed interface. The transmission rate can be up to a single 150MB / s. UPP send interface timing diagram and receive interface timing diagram is shown in Fig.6.

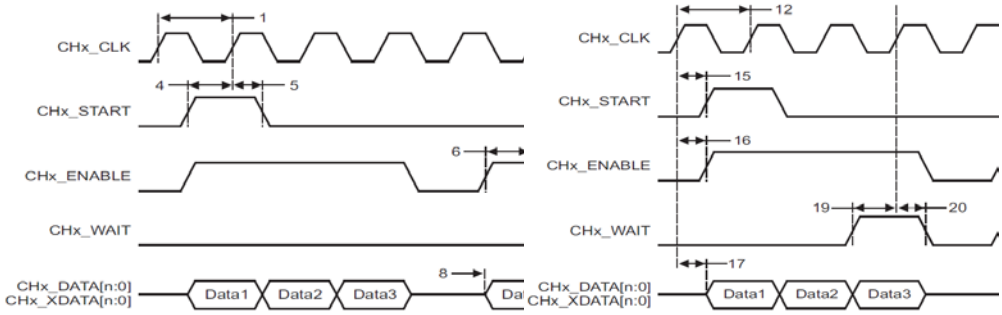

Fig.6.UPP receive mode (left) and UPP send mode (right)

When the UPP interface is configured for receive mode, the four signals except the WAIT signal are input signals. The WAIT signal can be controlled by the processor. When the UPP interface is configured for transmit mode, only the WAIT signal is the input signal and the other is the output signal. The processor will not be able to send data when the WAIT signal is pulled high, but also to disable the synchronization signal to ensure that the data transmission is waiting for the state until the WAIT signal is pulled down and continues normal transmission.

To ensure the real-time data problems, UPP interface with a single 75MB / S transfer rate.We should consider the asynchronous clock domain of the data in application. At the same time to ensure the correct transmission of data. Two asynchronous clock domains are added between an asynchronous fifo cache. The write data clock is 10MHz and the read data clock is 75MHz. Application for the asynchronous fifo to establish a cache mechanism, since the write clock is slow, fast read clock, we need FIFO to cache some of the data first. Wait for the amount of cache data to reach the set value and then allow the data to be read. When a row of data is read, the data is sent by the UPP to the DSP processor. UPP module and asynchronous FIFO module connection diagram is shown in Fig.7.

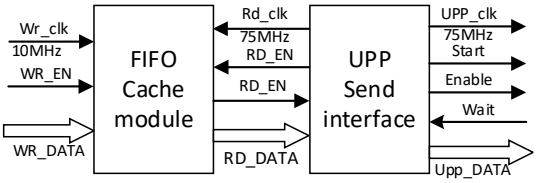

Fig.7.UPP logic module connection

UPP interface sending function through FPGA, according to UPP interface to send timing diagram, the synchronization signal ENABLE, the starting signal START as required to drive. The timing diagram of the UPP transmit logic is observed by the Signal Tap II logic analyzer. The UPP interface

sends the image data of the frame header 3AAA and 3AAB to the DSP processor. The timing diagram is shown in Fig.8.

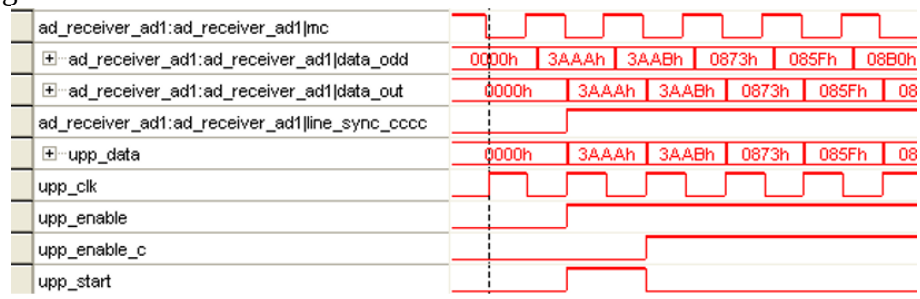

Fig.8.UPP interface send timing

UPP interface receive function through the DSP, using the CCS5.3 software's Memory Browser tool to view the image data stored in DDR3. When the data of the two processors is the same, the UPP interface receives the logic to work normally. The received data is shown in Fig.9.

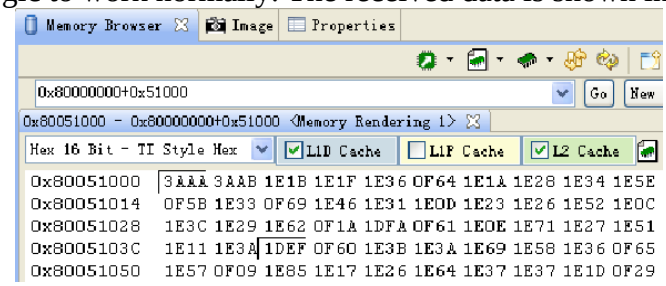

Fig.9.Receiving UPP image data of DSP storage

Power interface unit design

Power interface unit functions include two parts, the communication interface and power supply interface, as shown in Fig.10.

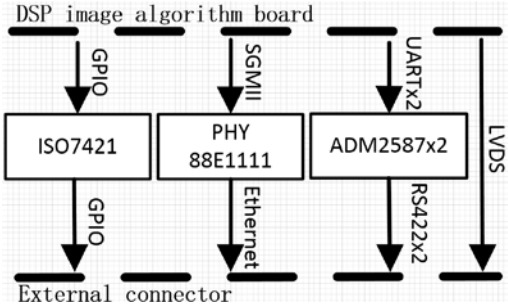

Fig.10.Power interface board diagram

The communication interface includes one Gigabit Ethernet, two RS-422, one IO and four pairs of LVDS signals. DSP image algorithm unit will be complex image algorithm after the data through the Gigabit Ethernet upload to the PC. Two RS-422 signals and one IO for external expansion communication. In addition, images that are not processed by complex image algorithms can be output directly through 4 pairs of LVDS. For the system to be able to be used in the UAV platform, the power supply is set at 28V ± 6V. So the design will reduce the input power to 9V, and then down to 5V and 3.3V, for other units to provide the necessary power.

System test

The uncooled LWIR image processing system is shown in Fig.11. The system transfers the final image data from the Ethernet to the system platform, the infrared image data is sent to the PC side using the UDP protocol. PC image receiving software displays the target tracking image, the video frame rate is 50fps as shown in Fig.12.

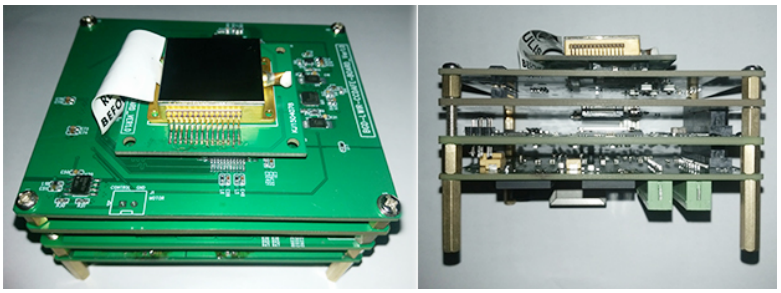

Fig.11. Uncooled LWIR image processing system

Fig.12.PC image receives the software interface

Conclusions

This paper designs an uncooled LWIR imaging processing system with TMS320C6657 DSP and EP3C25F324 FPGA processor as the core, and according to the system design requirements,we achieves the infrared image acquisition. At the same time according to the actual task needs to complete the image tracking, matching algorithms. Through a large number of experimental tests, at present the system has been applied to the UAV system platform.

References

[1]Suxia Xing,Junju Zhang,Benkang Chang.Infrared and Laser Engineering,2004,33: 441-444. “In Chinese”
[2]Suxia Xing.Study on Uncooled Infrared Thermal Imaging System [D]. Nanjing University of Science and Technology, 2005. “In Chinese”
[3]Lili Cang.Research on Uncooled Infrared Image Processing Technology Based on 384 × 288 Detector [J].Journal of Nanjing University of Science and Technology,2009. “In Chinese”
[4]ULIS. UL04371 - 042 640X480 VGA LWIR UNCOOLED MICROBOLOMETER[Z]. 2012.
[5]Na W. Design of uncooled focal plane array signal sampling using FPGA and AD9240[J]. China Medical Equipment,2010.
[6]Cheng Zhang,Feng Luo.Electronic Science and Technology,2011,24: 44-46.“In Chinese”