Reliability design of three mode redundant system based on dynamic reconfiguration[1]

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Keywords: MIPS, dynamic-reconfiguration, Markov process, triple-redundant

Abstract. In this paper, we design an improved three mode redundant self checking and self repairing system based on the technology of MIPS dynamic partial reconfiguration.The system adopts the fault tolerant model of reconfiguration and dual module comparison, The reliability of the system is analyzed by Markov process.The system is verified on the XUPV5-LX110T development board.

With the rapid development of electronic engineering and computer science, the limited hardware resources can not meet the needs of people.How to realize more functions on the limited hardware resources becomes the direction of people's exploration.Be based on FPGA（Field Programmable Gate Array）the research of dynamic local reconstruction technology for many years,The earliest is based on JBits　XC6200 Series FPGA Partial reconfiguration,But at that time, some of the reconfiguration capability is very limited,It is cumbersome and inconvenient to use [1].In 2005, a modular design method was developed,But the process is complex,And silicon chips are still very limited [1].Current XilinxAdvanced refactoring tools for refactoring PlanAhead,Partitions etc,Simple process,Easy to use.Be based on FPGA The reconfigurable technology has the characteristics of flexible and efficient hardware and programmable features,Dynamic system reconfiguration and static system reconfiguration.By the way of hardware information software,So that users can not only optimize the hardware and software can be changed and rewritten,Implementation of reconfigurable software chip in the form of bit stream.

With a wide variety of programmable logic devices in various fields to occupy an increasingly important position,Their fault tolerance has also been challenged by the high-tech industry.Aerospace,earthquake monitoring,Weather forecast,The traffic control and other industries have more and more requirements for the reliability of the equipment and the function of the operating system.Due to the special environment of high radiation,High vibration,damp,The impact of severe temperature changes and other unexpected events,Large computer communication equipment prone to software bit flow information dislocation or flip、All kinds of soft and hard errors. Traditional fault tolerant design does not use refactoring Technology,It is based on three mode or multimode redundant voting method,Can not fundamentally correct mistakes,Residual fault components can cause hidden trouble and waste of resources [2].How to process,Whole design,Function module design and internal structure design of the chip to improve the fault tolerance capability of the system,At present, it has become an important research topic in the field of high technology.

Would base FPGAAt present, the development of dynamic reconfiguration technology andfault-tolerant technology integration is thedevelopment direction of newAt present, many organizations have made some progress and achievements in the field of reconstruction technology.M1University of California Morphosys A coarse grain size、Reconfigurable structure with multiple files; M2 is M1Improved structure, Both DSPDevice flexibility and ASIC High performance chip [3].GarpOf the University of California at Berkeley BRASSResearch team

Developed,It is made up of a MIPS Microprocessor and FPGA Combined system[4]. FIPSOC is By SIDNA A coarse-grained structure is proposed in this paper FPGA The temporal logic part has

[1]Supported by the science and technology research project of Jiangxi Provincial Department of Education, in 2016.Project number is:GJJ161225.

the function of dynamic reconfiguration of multiple configuration files[5]. DPGA is Massachusetts Institute of Technology Transit Proposed project,Divided into two dimensional array elements DRFPGA[6],U.S.A Xilinx Corporate Virtex series FPGA is a typical fine granularity reconfigurable system. These results and the introduction of the product to the three modular redundant reconfigurable technology development to provide significant technical support. Paper in FPGA On the basis of the principle of dynamic partial reconfiguration,By adopting the fault tolerance model of three modules, an improved prototype of the self repairing system with three mode redundant self detection is designed and implemented,To ensure the safety and reliability of the system.

Design and Implementation

Overview of three modular redundancy system based on dynamic reconfiguration.

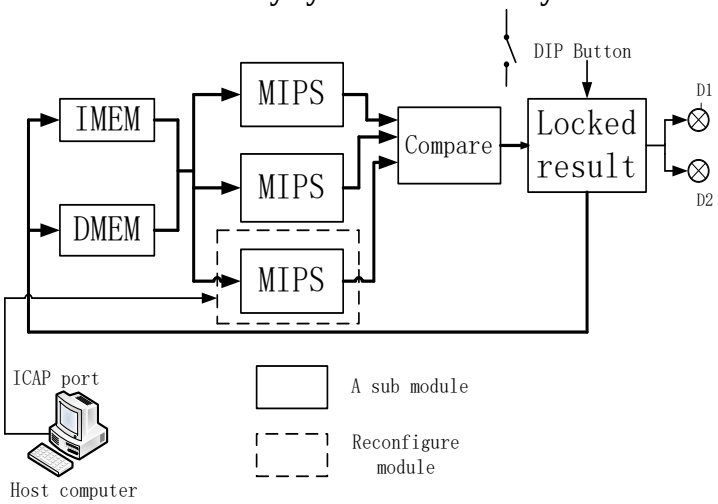

Figure .1.Three modular redundant system architecture based on dynamic reconfiguration

Figure 1 The overall structure of the system is given. In order to show the structure clearly, some modules are not drawn in detail, but it does not affect the understanding of the whole system. When the system fails，Dashed box MIPS（Microprocessor without interlocked piped stages）Abbreviation The subsystem will be restructured to FPGA Development board module, Does not cover the original MIPS subsystem. Such, Three MIPS subsystems can be compared to the results, the correct results. Figure 1 in the Host computer host computer is designed to download the main terminal equipment, complete the design of the entire system to generate a bit stream, Through the FPGA development board ICAP（Internal Configure Access Port）Configuration port will be generated to download the bit stream to the FPGA development board, to achieve the function of refactoring. D1 and D2 are two LED lights on the FPGA development board, the current calculation results are the same as the two MIPS modules, D1 light, or D1 lights, when the calculation results of 1, D2 lights, or D2 lights off. The main modules of the system are listed in table 1.

System module analysis.

Table 1 the main modules of the dynamic reconfiguration of three mode redundant system

Name	describe
IMEM（Instruction Memory）	Instruction storage
DMEM（Data Memory）	Data memory
MIPS	MIPS processor
Compare	comparator
Locked result	Result latch

It should be noted that, in order to ensure that the bitstream can be downloaded, The MIPS processor does not contain instruction memory and data memory, and the instruction memory and data memory are connected in the form of an instantiated IP core.

Instruction memory is used to store instructions when the system is in operation, and the data memory is used to store the final result of instruction execution. The comparison module is used to compare the two sets of data from the MIPS processor, and the output of the current two MIPS

processors is the same, One of the results directly into the Locked result, When the data of the two groups are not the same, the third MIPS processor in reconstruction, and then output three MIPS processor to compare the results, two of which the same result can be identified as correct results, it is stored in Locked result. The Locked result module is used to lock the value of the output, and the correct results calculated by MIPS will be temporarily stored here. Of course, the output of the system will be stored in the data memory.

Results the storage structure consists of data memory RAM or trigger. This design can easily realize data storage with a dual port RAM: let write data address RAM (here as a data storage address at the beginning of the 0 storage). The system clock is connected with the RAM clock, the data storage interface is connected with the RAM write data port and the storage condition interface is connected with the RAM write enable port. When the system clock edge comes, if the storage conditions are valid, that is, when the write enable RAM is valid, the data written into the data entry into the RAM to complete the data storage. The following code for data storage clock:

```
assignclk = (~(|pc))&(~(|data_in[31:1]))&data_in[0];
/*Should generate a rising pulse, the design calculation results for 1*/
```

MIPS microprocessor analysis

MIPS processor has three kinds of micro structure: single cycle, multi cycle and pipeline. They differ in the number of storage components and the number of non - Architecture storage components. Three kinds of micro structure of MIPS processor are register, ALU, finite state machine, memory and other logic module and so on. The same microprocessor architecture can have different microstructures, resulting in different trade-offs in performance, cost, and complexity. They can run the same program, but the interior design is very different. The MIPS processor designed in this paper is based on a single cycle MIPS processor, but it does not contain the instruction memory and data memory.

MIPS internal structure.

Figure 2 is the internal structure of the MIPS processor, in order to clearly indicate its structure, the connection between some modules is not drawn in detail.

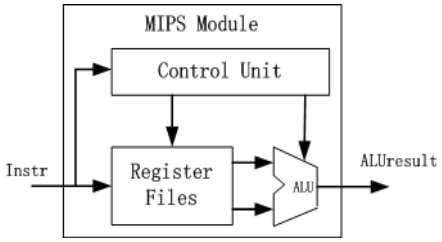

Figure. 2. MIPS internal structure

As can be seen from Figure 2, the MIPS processor consists of three modules: the control unit, the register file unit, and the computing unit. The control unit for each MIPS module in the opcode field and the function field in the instruction is calculated based on the control signal, the register file unit is used for data acquisition and storage, ALU unit will read from the register data processing, R type arithmetic / logic instructions can be completed（add，sub，and，or，slt），Memory access instruction（lw，sw）and Branch instruction （beq，bnq）Calculation, The calculated results are sent to the data store for storage or as the input address of the register file unit. The fault tolerant system consists of three identical MIPS processor modules. The processor obtains instructions from the instruction memory according to the PC value, and then sends them to the two input ports of the MIPS module in the running state. Each instruction is composed of several different fields.

Introduction of instruction set.

Simple design helps to make a regular, and the most common choice is to encode the instructions into words stored in memory. Although some instructions may not require all 32 bit coding, variable length instructions will greatly increase the complexity. The instruction set of the MIPS processor architecture uses a 32 bit instruction structure that defines the three instruction formats: R- type, I- type and J- type. A small amount of instruction format allows for a variety of custom designs that

can be applied to a variety of formats, so the hardware can be simple and applicable to different commands. Table 2 gives a detailed description of the three instruction formats. R- type instruction format, I- type instruction format, J- type instruction format [7].

Table 2 MIPS instruction set format[7]

R-type	op(6 bits)	rs(5bits)	rt(5 bits))	rd(5 bits)	shamt(5 bits)	funct(6 bits)
I-type	op(6 bits)	rs(5 bits)	rt(5 bits)	imm(16 bits)		
J-type	op(6 bits)	addr(26 bits)				

The R-type instruction has three register operands, two for the source operand, and one for the destination operand. The command code is divided into two sections: OP and funct. The instruction operand code is divided into three fields: RS, RT and RD, the first two registers RS and RT are the source registers, and the RD is the destination register. The fifth field shamt is used only for the shift operation, and the 5 bit binary value stored in the shamt field represents the number of bits, for other commands, shamt is 0.

The I-type instruction has two register operands and an immediate operand number. This 32 bit instruction has 4 fields, namely OP, RS, RT and imm. OP is the instruction opcode field, RS, RT, and IMM are instructions for the operation of the digital segment. RS and IMM are used as source operands, in some instructions (such as addi and LW), RT is used as the destination operand, and in other instructions (e.g. SW), RT is also used as the source operand. The first three fields (OP, RS, and RT) have the same number as the R-type command. The Imm field represents a 16 digit number.

The J-type instruction format is used only for jump instruction, which has a 26 bit address operand addr for the specified address. As with other instruction formats, the preceding 6 bit OP is the opcode field.

The instructions of the operation code for the OP and funct, to determine the operation and storage of ALU units.

Conclusion

In this paper, we do some exploratory work on the control of the multi-mode redundancy and the reliability of the control network. Unlike other design, the design adopts self repair mode to realize the dynamic reconfiguration system, without error module of long-term residual, saves chip space, improve chip utilization, ensure the system accuracy.

References

[1]Wenjie Zhang Simulation of an anti delay communication algorithm in process control network. computer simulation[J],2014.04

[2] M.H.Lee, H.Singh, G.Lu, N.Bagherzadeh, F.J.Kurdahi. “Design and Implementation of the Morphosys Reconfigurable Computing Processor”, Journal of VLSI Signal Processing Systems, vol.24, pp.164-172, March 2000.

[3] Callahan.T.J, Hauser.J.R, Wawrzynek.J. The Garparchitecture and C compiler. IEEE Comput. Soc. Vol.33(4), p 9-62, April 2000.

[4] Moreno.J.M, Canto.E,Cabestany.J, Faura.J, Lacadena.I, Insenser.J.M.“Rapid prototyping of electronic systems using FIPSOC”, 1999 7th IEEE International Conference on Emerging Technologies and Factory Automation. Proceedings ETFA '99 (Cat. No.99TH8467), p 287-96 vol.1, 1999.

[5] DeHon,A.“DPGA-coupled microprocessors: commodity ICs for the early 21st Century”, Proceedings IEEE Workshop on FPGAs for Custom Computing Machines (Cat. No.94TH0611-4). P 9-31, 1994.

[6] David Money Harris, Sarah L.Harris.Digital Design and Computer Architecture.China Machine Press. Beijing. P299-304, P363-461, 2007

[7] Jinfeng Li, Huanle Zhu, Wenjie Zhang. Application study of project drivers in "electronic circuit design and simulation" in classroom teaching[J]. Journal of bosom friend inspiration, 2016.04.

[8] Jinfeng Li, Wenjie Zhang. Professional quality of preparatory teachers in the classroom under the new situation[J]. Journal of hundreds prose, 2015.06.