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Core Power Design of High Performance DSP and Its Voltage Ripple Suppression

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***Abstract*—Aiming at the low voltage, high current and low voltage ripple demand of 100G DSP, this paper presents a power design using LTM4650 as the core device. Analyzing the causes and influencing factors of voltage ripple, a solution that used multi-phase parallel and the low ESR capacitor was applied, to suppress the voltage ripple. The results of LTspice simulation software and the actual circuit test, proved that the power design can meet the power requirements of 100G DSP and is able to guarantee the stability of the DSP system.**

Keywords-LTM4650; switching power; ripple suppression

I. INTRODUCTION

With the development of optical fiber communication technology and the use of complex modulation method and coding format, digital signal processor (DSP) plays a key role in the signal processing of high speed optical transmission system. The power supply is the basis of DSP system design, which is also essential and critical.

In order to get a reliable power design, the following issues must be considered: (1) the upper and lower limit of load current, (2) output voltage ripple, (3) circuit space (4) power sequence (5) electromagnetic compatibility etc. [1].

This paper presents a power design of high performance DSP, which ensures the stability of DSP system through simulation and actual testing of output voltage and its ripple.

II. ANALYSIS OF CORE POWER DEMAND

The high-performance 100G DSP is a large-scale integrated circuit based on digital coherent detection technology, which is the key to build 100G ultra-high speed and long distance digital optical transmission system. A series of complex digital algorithms in digital coherent detection technology, such as, clock recovery, dispersion compensation [2], are all performed in the 100G DSP. Therefore, it requires a high-performance power supply as a guarantee.

TABLE I. 100G DSP RECOMMENDED OPERATING CONDITIONS

Power (V)	Function	Voltage Range (V)			Current (A)
		Min	*Typ*	*Max*	
0.875	Core Power	0.825	0.875	0.925	71.28
0.9	SFI-S ADC	0.86	0.9	0.99	8.04
1.8	IO Power	1.65	1.8	1.95	1.40

Power of 100G DSP mainly include 0.875V core power supply, 0.9V ADC, SFI-S power supply and 1.8V IO power supply, the specific parameters of which are in Table I[3]. The design of power supply must be strictly in accordance with the recommended working conditions in Table I, so as to ensure the safe and stable use of 100G DSP.

III. CORE POWER DESIGN

As can be seen from Table I, core power of 100G DSP is 0.875V, and its minimum and maximum values are 0.825V and 0.925V respectively. The voltage fluctuation of core power is required to be within 0.1V, and the output current is up to 71.28A at full load. Therefore, the LDO power supply is unable to meet the demand, while the switching power supply is the best choice. The voltage ripple of switching power is generally quite high, so voltage ripple rejection must be taken into consideration in the design of the core power to meet the power requirements of 100G DSP.

A. Device Selection

Aiming at the 100G DSP's characteristics of high current and low voltage ripple, taking into account the actual circuit space constraints, finally select LINEAR μModule LTM4650 as the core device.

The LTM4650 is a dual 25A or single 50A output switching mode step-down DC/DC μModule (power module) regulator. Included in the package are the switching controllers, power FETs, inductors, and all supporting components. The main advantage of the device is its precise current architecture, which is able to achieve current sharing in multi-phase mode, so the output current of two paralleled devices can be up to 100A. And the device also has features like, small package (16mm * 16mm * 5.01mm), good heat dissipation, which is able to meet the actual circuit requirements of 100G DSP.

B. Power Structure Design

For high-power, high-current switching power, the use of multi-phase parallel can suppress the voltage ripple to a certain extent. The basic theory is as follows. Take paralleled two-channel switching power as an example (Figure I), Both DC1 and DC2 can provide output power and generate voltage ripple, meanwhile. Assuming that the duty cycle of the two channels is 50% and adjusting the phase difference of ripple to 180°, by paralleling the output of the two channels, the voltage fluctuation can be reduced and the voltage ripple will be

significantly restrained, which contribute to the improvement of power performance [4].

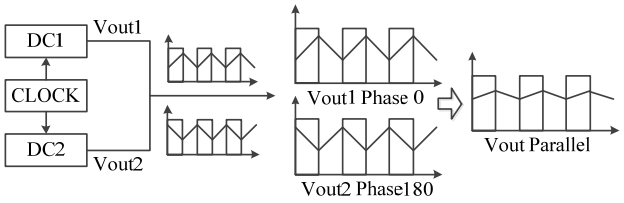

FIGURE I. BASIC PRINCIPLE OF DUAL CHANNEL VOLTAGE RIPPLE SUPPRESSION

For LTM4650, changing the PHASMD pin level (Table II) will make the CLKOUT pin to output different clocks with several diverse phases

TABLE II. PHASMD PIN LEVEL VS CLKOUT PHASE

PHASMD Pin Level	***SGND***	***FLOAT***	***INTVcc***
CLKOUT Phase	60°	90°	120°

The other LTM4650 can receive the clock through the MODE_PLLIN pin and use the internal PLL to synchronize the switching frequency so that the output voltage reaches the corresponding phase.

LTM4650 is able to support up to 12 paralleled channels in multi-phase mode, and the output current can be up to 300 A. According to the actual requirements, the scheme using 4 paralleled channels, output current of which is up to 100A, can meet the demand, as shown in Figure II. The output phase of the first LTM4650 is 0° and 180°, respectively, and the output phase of the second LTM4650 is 90° and 270°, respectively. Theoretically, in multi-phase mode, voltage ripple of 4 paralleled channels can be reduced to a quarter.

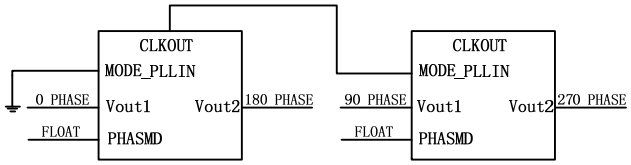

FIGURE II. SCHEMATIC OF LTM4650 FOUR-PHASE

C. Peripheral Circuit Design

After determination of the power's four-phase parallel structure, it is required to configure the output voltage V_{out}, switching frequency f_s, output capacitor C_{out}, input capacitor C_{in} and other parameters.

1) The output voltage can be determined by the resistor divider connected between the V_{fb} pin and the ground pin. For the calculation method, see (1)

$$V_{out}=0.6\text{V}\times\frac{60.4k+R_{fb}}{R_{fb}} \quad . \tag{1}$$

For paralleled connection in multi-phase mode, a common voltage setting resistor can be used, while the output channels are required to connect to the same feedback loop. According to the core power requirements of 100G DSP, using (1) to calculate R_{fb}=133 kΩ, when V_{out}=0.875V. The switching frequency f_s is determined by the voltage of the Fset pin, as shown in Figure III.

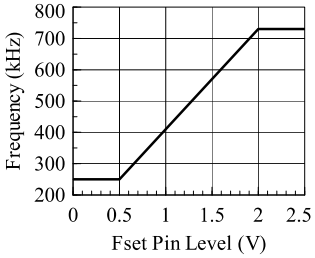

FIGURE III. SWITCHING FREQUENCY VS FSET PIN VOLTAGE

Selecting an appropriate switching frequency can improve the energy conversion efficiency and LINEAR official recommended frequency is shown in Table III.

TABLE III. RECOMMENDED FREQUENCY

Output Voltage (V)	***1.0<***	***1.0-1.5***	***>1.5***
Switching Frequency (kHz)	400	500	600

Since the core voltage is 0.875V, according to Table III, setting switching frequency to 400kHz, the efficiency of power can achieve the desired efficiency. In Figure III, 400kHz corresponds to about 1.0V. For the reason that the Fset pin has a constant current source of 10uA, the switching frequency (400kHz) can be determined by connecting a 100 kΩ resistor to the Fset pin in series, according to Ohm's law.

2) The output capacitor should have a low equivalent series resistance (ESR) to achieve lower voltage ripple and better power stability. Considering the extreme case, for the step load, the selection of output capacitor can refer to (2):

$$C_{out}\geq\frac{I_{step}}{(\Delta V_{out}-I_{step}\times ESR)(f_s/V_{out})} \quad . \tag{2}$$

ΔV_{out} is the output peak-to-peak voltage and I_{step} is the step load. For 12V input and 0.875V output, voltage ripple is required to be less than 100mV. Assuming ESR=50 mΩ, f_s=400kHz, C_{out} can be calculated as 510uF, which indicate the output capacitance of each channel should be at least 510uF.

For better filtering, it is better to increase the number of output capacitors.

3) The input capacitor C_{in} is used to reduce the ripple of the input voltage. If the system requires a small input voltage ripple ΔV_{in} , C_{in} can be calculated using (3):.

$$C_{in} \geq \frac{I_{out} \times D(1-D)}{f_s \times \Delta V_{in}} \quad . \tag{3}$$

I_{out} is the maximum output current, ΔV_{in} is the input peak to peak voltage ripple, D is the ratio of output voltage to the input voltage. In this design, I_{out} =71.28A, D =0.073, f_s =400kHz, ΔV_{in} =200mV, taking these parameters into (3). C_{in} can be calculated as 60.25uF, so, at least three 22uF capacitor should be used in parallel for each input channel.

IV. Simulation of Power Design

A. *Causes and Influencing Factors of Voltage Ripple*

Figure IV shows the simplified schematic diagram of Buck switching power, which is mainly comprised of switching controller, inductors, capacitors, fast recovery diodes and other components.

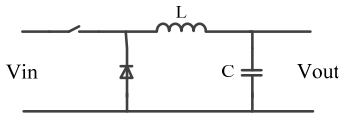

FIGURE IV. SIMPLIFIED SCHEMATIC OF BUCK SWITCHING POWER

Switching controller switches at high-speed under the control of PWM wave, which will produce the output voltage fluctuations, and the introduction of voltage ripple at the same frequency in circuits. The inductor of output circuit will induce leakage inductance, the reverse recovery current of output diode can also cause current spikes. In the actual circuit, there will be various forms of parasitic inductance between the wires or between the power pins, which will also introduce noise [5]. Calculation of voltage ripple can refer to (4), Where L and C represent the inductance and capacitance respectively, in the switching power.

$$\Delta V_{out} = \frac{V_{out}(1-D)}{f_s L}\left(ESR + \frac{1}{8 f_s C}\right) \quad . \tag{4}$$

Firstly, analyze the mathematical expression with in latter brackets of (4):

$$ESR + 1/8 f_s C \quad . \tag{5}$$

Selecting a set of typical values: f_s = 400 kHz, C = 470uF, $1/8 f_s C$ is calculated as 0.66 mΩ . Generally for the output capacitor, ESR of several paralleled ceramic capacitors and electrolytic capacitors is around ten milliohm. It can be seen that the ESR of the output capacitor has a more pronounced effect on the voltage ripple.

Secondly, analyze the mathematical expression with in former brackets of (4):

$$\frac{V_{out}(1-D)}{f_s L} \quad . \tag{6}$$

Increasing the switching frequency f_s or increasing the inductance L can reduce the voltage ripple. But the increase of f_s will result to increased power consumption, and the inductance L is LTM4650 internal integration, which can't be changed. Therefore, voltage ripple suppression is achieved mainly by selecting appropriate output capacitor, the ESR of which is lower.

B. *Simulation of Ideal Design without Considering ESR*

In ideal situation, schematic of Buck-switching power is shown in Figure IV, where ESR of capacitor C is 0 mΩ . The voltage ripple is generated only by the switching controller. Utilizing LINEAR's software LTspice to do simulation with parameters as follows: V_{in} =12V, V_{out} =0.875V, f_s =400kHz, three 22uF input capacitor, a 220uF and a 33uF capacitor.

According to (4), the calculated voltage ripple is 9.6mV, for four-phase switching power, the ripple will be reduced to a quarter of original, so the final voltage ripple is 2.4mV. The simulation results are shown in Figure V.

As seen in Figure V, voltage ripple is approximately 2mV, which is close to the theoretical calculated value.

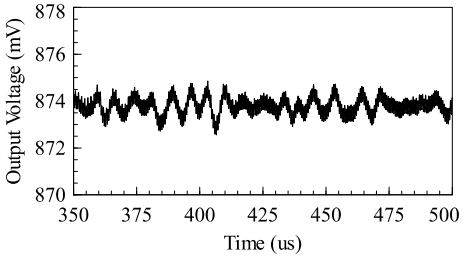

FIGURE V. SIMULATION OF IDEAL DESIGN WITHOUT CONSIDERING ESR

C. *Simulation of Actual Design Considering ESR*

In the actual circuit, due to poor electrical connection and electrolyte drying and other reasons, the capacitor ESR will become higher, and then introduce a larger voltage ripple. Now only change parameters of the output capacitor, and discuss the scheme:

1) Two 100uF (ESR=25 mΩ) ceramic capacitors and one 330uF (ESR=50 mΩ) tantalum capacitor were selected. The simulation results are shown in Figure VI

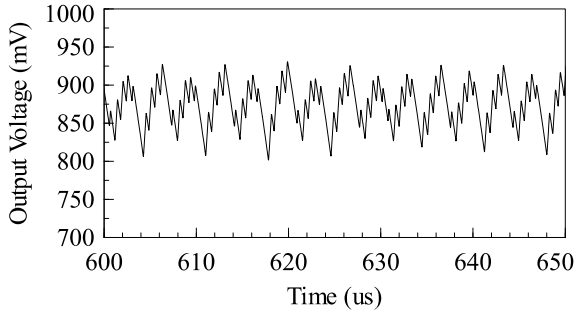

FIGURE VI. SIMULATION RESULTS OF ORDINARY CAPACITORS

As can be seen from Figure VI. The output voltage fluctuates between 800mV and 940mV and the voltage ripple is about 140mV, exceeding the recommended operating range of the 100G DSP.

2) Two 220uF (ESR=12 mΩ) ceramic capacitors and one 470uF (ESR=15 mΩ) tantalum capacitor were selected, the ESR of which is lower, while the capacitance of which is higher. The simulation results are shown in Figure VII.

Using capacitors of better quality, the voltage ripple is significantly reduced and the output voltage fluctuates between 868 mV and 880 mV. The voltage ripple is about 12 mV, fully meeting the power requirements of 100G DSP.

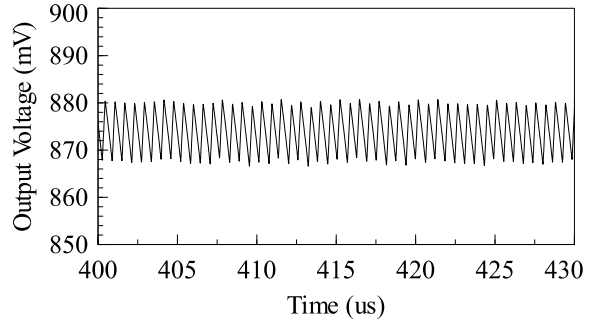

FIGURE VII. SIMULATION RESULTS OF LOW ESR CAPACITOR

V. ACTUAL TEST OF CORE POWER

A. Voltage Ripple of Ordinary Capacitor

In the actual test, two 100uF (ESR=25 mΩ) tantalum capacitors and one 330uF (ESR=50 mΩ) tantalum capacitor were selected as the output capacitor. Oscilloscope AC coupling test results shown in Figure VIII, the voltage ripple is about 175mV, which is greater than simulation results that is 140mV. The reason may be that the welding resistance and resistance introduced through the hole can't be ignored in the actual circuit, resulting in increased ESR and increased voltage ripple.

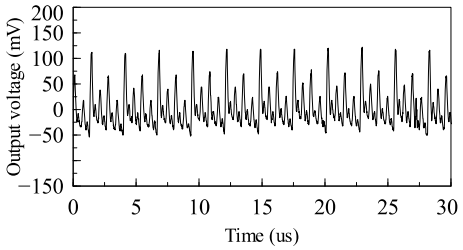

FIGURE VIII. TEST RESULTS OF ORDINARY CAPACITORS

B. Voltage Ripple of Low ESR Capacitor

Two 220uF (ESR=12 mΩ) tantalum capacitors and one 470uF (ESR=12 mΩ) tantalum capacitor were selected. The test results are shown in Figure IX. Voltage ripple is about 15 mV, close to the simulation results, which meet the power requirements.

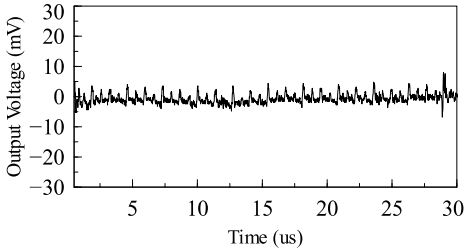

FIGURE IX. TEST RESULTS OF LOW ESR CAPACITOR

VI. CONCLUSION

According to the power requirements of 100G DSP, this paper presents a power design that use LTM4650 as the core device. The Use of multi-phase parallel method and low ESR capacitor contribute to suppression of the voltage ripple. Through the simulation and the actual test, performance of the power design is verified and is able to meet the 100G DSP's demand of low voltage, high current, low voltage ripple, which ensure the stability and performance of the DSP system.

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