

Electronic Perpetual Calendar Design Based on CPLD

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Abstract. The design method of electronic perpetual calendar is discussed in this paper. And the design is finished by VHDL language. The hardware model of the system is simple, and the system has high precision and dependability. Finally the program is accomplished and downloaded into CPLD chip named MAXII-EMP1270T144C5.

Introduction

With the rapid development and popularization of science and technology in recent years, our work and life concept has also undergone tremendous changes. The demand for all kinds of electronic products is getting higher and higher, so that the electronic perpetual calendar closely related to life is becoming more and more intelligent To facilitate. People will buy a new calendar in every new year, accompanied by a picture of the calendar card hanging on the wall, both decoration, but also to indicate the year, month, day, week and other information. But the use of this paper calendar, you must remember to tear a day on time, otherwise it will remember the wrong date, often because people forget to tear every day and remember the wrong date, missed important things, causing losses. Compared with the traditional paper calendar, electronic calendar has been more and more widely used.

The design based on FPGA chip, the external circuit is simple, the system integration is high, high precision, the use of VHDL programming language, the way the software design hardware, flexibility, easy to upgrade after the product [1].

System Design.

According to the requirements of the system design function, the system can be divided into four modules: integrated timing module, data adjustment module, keyboard acquisition module and digital display module. The integrated time module includes seven sub-modules, each of which must have preset , Count and carry function, the system block diagram is as follows:

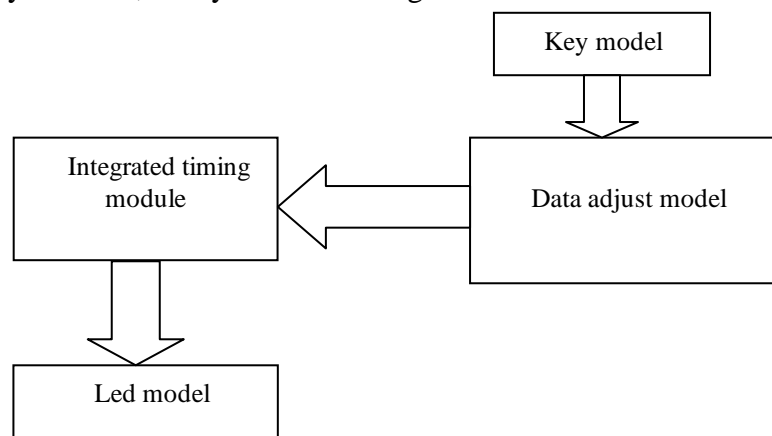


Figure 1. System function module diagram

Specific Module Design

Integrated Timing Module. The integrated chronograph module is divided into seven sub-modules, such as the counting module, the scoring module, the time module, the metering module, the counting module, the monthly module and the year module. The seven sub-modules have preset, count and carry function, Design ideas are as follows:

(a) count the second module: the second pulse as the count clock circuit count clock signal, to be counted to 60 moments, carry, score circuit plus 1, while the second circuit is cleared and re-seconds.

(b) scoring module, timing module: its design ideas and the second module is similar.

(c) the program week module: the timing circuit generated by the carry pulse signal as the metering module count clock signal, to be counted to 6 moments, the week module returns 0 to start counting again.

(d) the date module: the timing module generated by the carry pulse signal as the counting module count clock signal, through the system to determine the total number of days this month X (including 28,29,30,31 four cases), to be counted To X + 1 instant, carry, the month module plus 1, and the date module returns 1 to start counting again.

(e) the month module: the counting module generated by the carry pulse signal as the monthly module count clock signal, to be counted to 12 instant, carry, year module plus 1, and the month module returns 1 to start counting again.

(f) year module: the month module generated by the carry pulse signal as the count module clock signal, to be counted to 100 moments, the year module returns 0 to start counting again.

The following to the daily module, for example, the system simulation, simulation diagram is as follows:

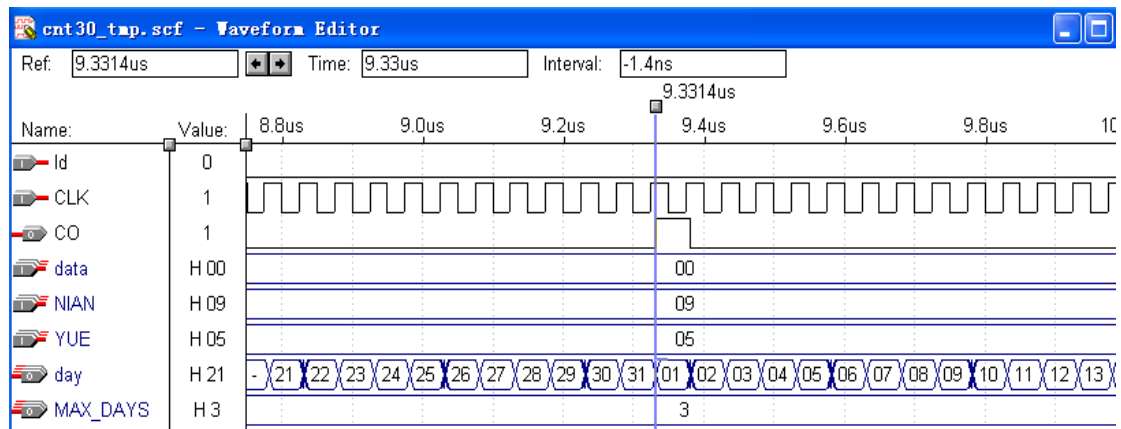


Figure 2. Simulation of the daily module

The above is the May 2009 module simulation, from the simulation we can see, 31 days in May, MAX_DAYS with "11" to represent the back of the module, The main program code is as follows [2]:

```

if ld='1' then day<=data;
elsif CLK'EVENT AND CLK='1' THEN
case max_days is
when "00"=> --28 days
if day(7 downto 5)="000" then
if day(3 downto 0)="1001" then
day(3 downto 0)<="0000"; day(7 downto 4)<=day(7 downto 4)+1;
else day(3 downto 0)<=day(3 downto 0)+1;
end if;
co<='0';

```

```

elseif day(7 downto 4)>="0010" then
if day(3 downto 0)>="1000" then
day(3 downto 0)<="0001"; day(7 downto 4)<="0000";co<='1';
else day(3 downto 0)<=day(3 downto 0)+1;co<='0';
end if;
else null; end if;
when "01"=>--29 days
...
when "10"=>--30 days
...
when others=>--31 days
...
End case;
End if;

```

Data Adjustment Module. For the system to adjust the data module, mainly through the modal key and adjust the key to complete. Mode key is responsible for switching the normal time count mode and time adjustment mode, adjust the mode switching sequence shown in Fig.3. The adjustment key is responsible for adjusting the timing of the current mode under the time adjustment mode. The module uses a state machine to complete.

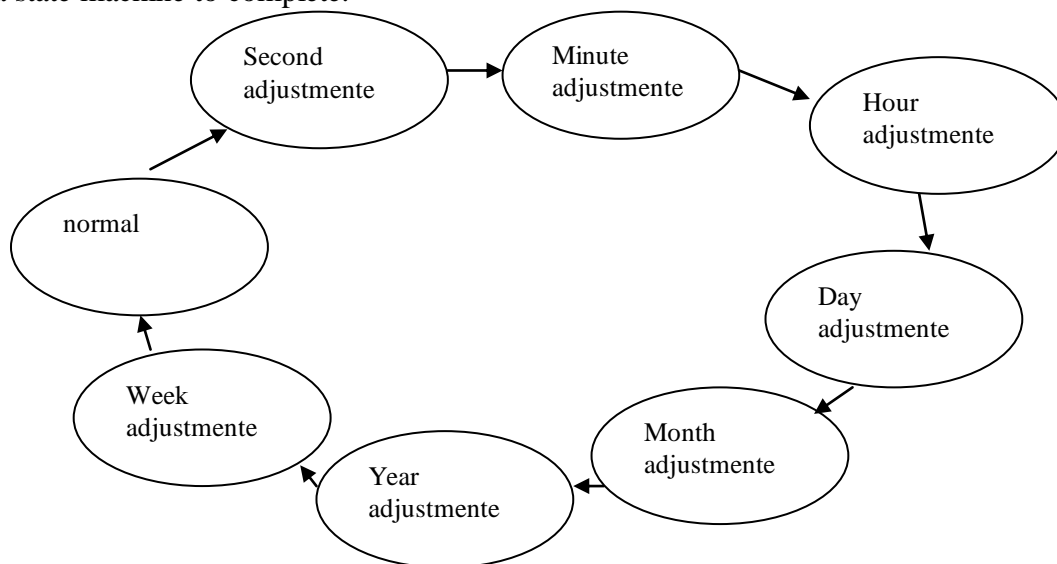


Figure 3. Adjust the mode switching sequence

Digital Display Module. The system used a total of eight digital control to complete the display, the data to be displayed divided into two groups, year, month, day group, week, hours, minutes, seconds a group, through the keyboard to select control. The interface of the module is as follows:

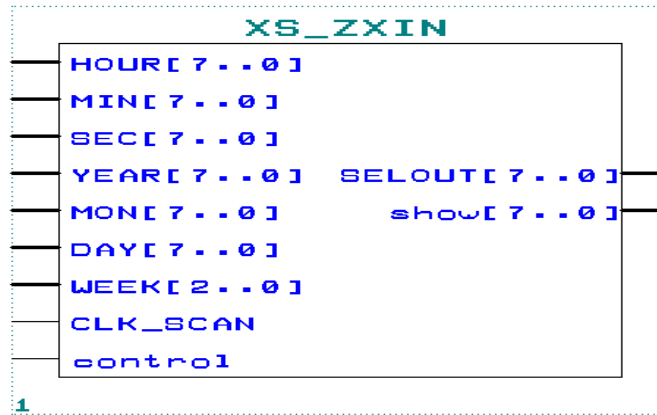


Figure 4. digital tube display module diagram

Summary

This design is downloaded to the target chip EPM1270T144C5, the entire system is stable, high timing accuracy, from the comprehensive report shows that the higher utilization of resources.

The innovation of this paper: the use of CPLD to achieve electronic calendar, the external circuit is simple, a high degree of system integration, design flexibility, accuracy is also significantly higher than the ordinary electronic calendar.

References

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- [2] Shen Ming Shan. EDA technology and programmable device application training [M]. Beijing: Science Press, 2006: 223-224.