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Embedded Children Painting Machine Based on Image Processing

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***Abstract*—According to the characteristics of children's early paintings, this paper designed a kind of hardware and software system based on FPGA and ARM dual-core architecture, the system realizes the physical image contour extraction, display, enhancement. And can through the SD card to store image and use network to connect the printer to print, which enhance children's cognition of the object and train the ability of painting.**

Keywords-embedded; children painting machine; image processing

I. INTRODUCTION

Children painting education as a kind of children's early intelligence and potential development, an effective way to cultivate children's imagination and creativity, has been known and paid more and more attention[1]. But the children's understanding of the "three-dimensional, space" is not enough, for the children's painting is more symbolic for a single image. Children painting machine simplify object characteristics, highlight the outer contour and make children easily identifying, which help children establish a creative way of thinking. It will be a great help to the development of children's painting.

II. CHILDREN PAINTING MACHINE

A. *Structuer and Principle*

The children painting machine based on FPGA and ARM dual-core hardware system architecture, as shown in FIGURE I. The FPGA is EP2C70, mainly realize the infrared signal reception and objects image acquisition, identification, handling, etc. The ARM is S3C641O, mainly used for the image store to SD card, network communication, LCD display, etc. Two modules' high-speed data transmitted via SRAM[2].

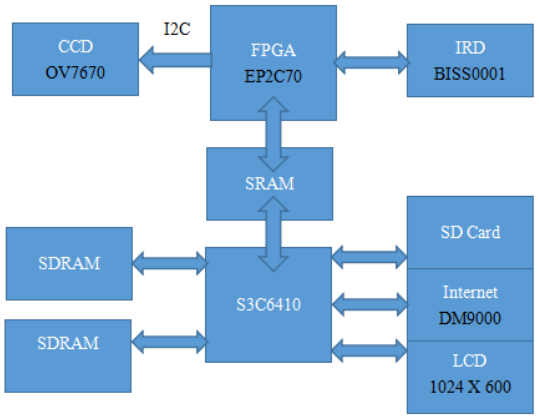


FIGURE I. DUAL-CORE HARDWARE SYSTEM ARCHITECTURE

Infrared sensors installed in the front drawing machine, used to detect the children and the distance to the screen, in order to protect the eyesight. When the distance is too close the screen becomes green leaves to remind children should keep their distance. A CCD is installed behind the painting machine. The CCD real-time display objects and by touching LCD screen buttons commands are sent to acquire the object's imagination. The image contour is extracted and displayed when triggered by the function keys. The whole process display on the LCD[3] .Through the VGA or HDMI interface module the imagination can be shown to the computer and TV.

With Samsung S3C6410 ARM11 controller as the core, two pieces of SDRAM used to data exchange and the SD Card to image storage. DM9000 used to implement the function of Ethernet. The LCD connected through the bus. The system design a FLASH to run Linux kernel - 2.6.36 operating system, realize the interaction and control the whole system function. In the system level, transplant BootLoader1. 12 version, using arm - Linux - GCC cross-compilation; For Linux system 2. 6 version of the kernel cutting[4], compilation, transplantation, and file systems, such as: increase the systems required for a variety of peripheral module driver.

B. *Software Design*

Firstly, according to the signal hardware process as shown in FIGURE II, the software is divided into three parts: signal acquisition, processing and output. Image input for CVBS composite signal, establish corresponding module to read and BT656 decoding[5], as shown in FIGURE III.

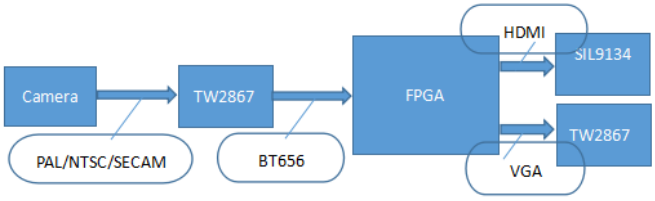


FIGURE II. SIGNAL HARDWARE PROCESS

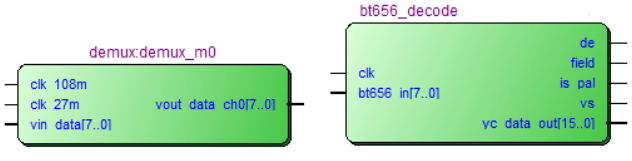


FIGURE III. BT656 DECODE

As a real-time processing, SDRAM as a frame buffer, equivalent to a FIFO, images from CMOS constantly come in, and then after SDRAM out by VGA[6]. In FPGA by the trigger can be determined on a moment with a moment of data changes, thus create the Line buffer can well solve the problem of pixel information. As shown in FIGURE IV, through the Mega Wizard create a Shift Register module, assuming that the image is 640 x 480, so the line buffer length of only 640 would be enough.

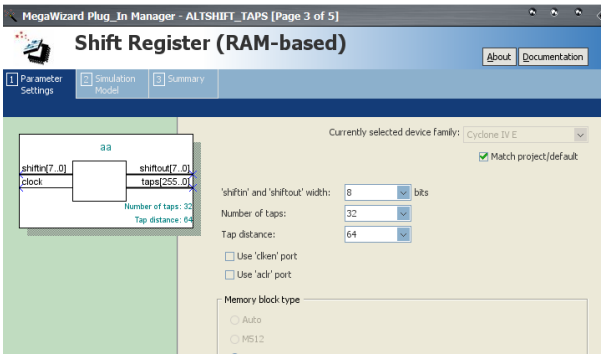


FIGURE IV. SHIFT REGISTER MODULES

```
Define LineBuffer_1 b1 (
clken(iDVAL),.clock(iCLK),
shiftin(iDATA［9:2］),
.taps0x(Line0),
.taps1x(Line1),
.taps2x(Line2));
```

Sobel edge detection with Gx Gy in the X direction, Y direction with a central pixel of the convolution operation [7].As shown in FIGURE V line buffer operation diagram, three line buffer using Megafunction altshift_tab completion, and Gx take part completed by altmult_add and parallel_add Megafunction.

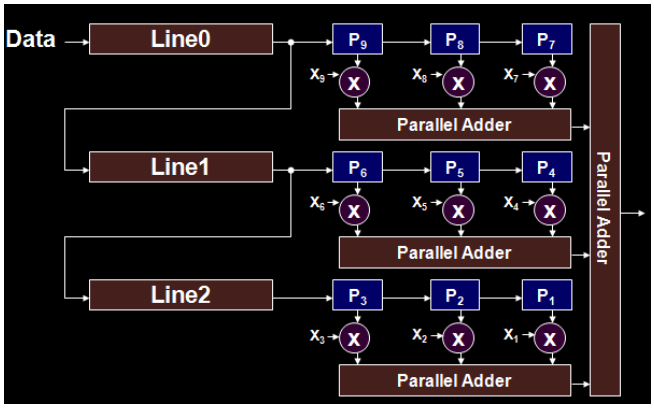


FIGURE V. LINE BUFFER OPERATION DIAGRAM

SOBEL algorithm, the definition and algorithm of concrete[8] block diagram is shown in FIGURE VI.For the valve value judgment is adopted:

```
assign oDATA=(Abs_mag > iTHRES_Hold) 0 : 1023;
```

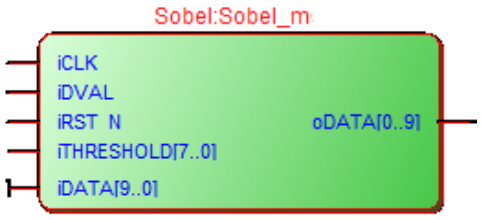


FIGURE VI. SOBEL ALGORITHM BLOCK

Images transmitted from FPGA to ARM and used for SD card storage software processing are shown in FIGURE VII below:

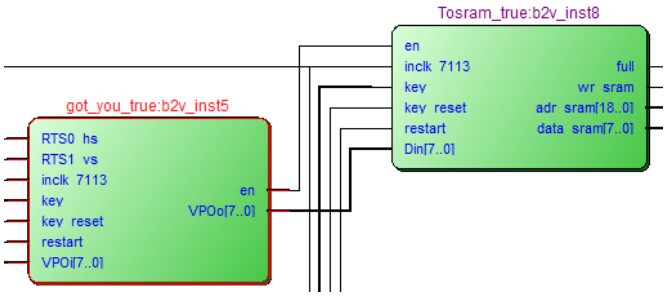


FIGURE VII. DATA TRANSMISSION AND STORAGE

Through the Signal Tap II Logic Analyzer on-line monitoring data acquisition and processing after the changes, as shown in FIGURE III:

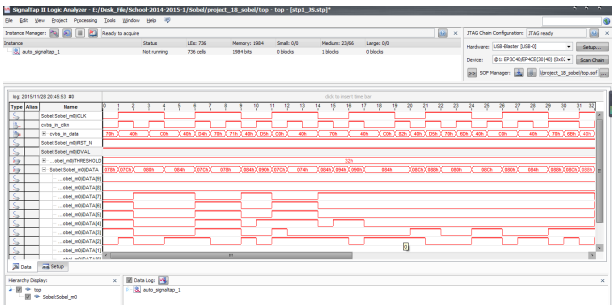
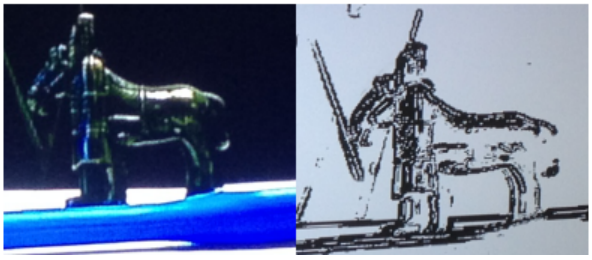


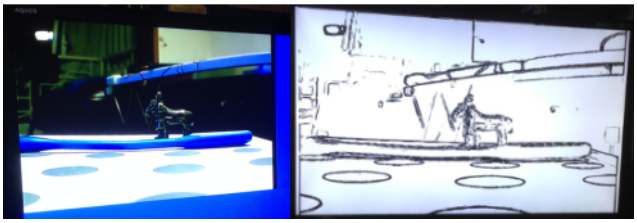
FIGURE VIII. REAL-TIME IMAGE DATA GATHERING AND EXAMINATION

Finally, through the program algorithm processing, good results are shown in FIGURE IX and X. Figure IX A and X A is the original image, FIGURE IX Band X B for algorithm processing figure. It is better recognize and easily paint the edge feature for the processing image.



A. Original Image *B.* Processed Image

FIGURE IX. IMAGE COMPARISON



A. Original Image *B. Processed Image*

FIGURE X. IMAGE COMPARISON

III. CONCLUSION

A Dual-core architecture of children drawing machine in the aspect of image processing effect is remarkable, shown in FIGURE XI. It deepen children's perceptions of the beautiful things and cognitive level, cultivate children's aesthetic ability so as to let them know themselves better and more confident and creative expression. As the picture show below, seeing is painting.

FIGURE XI. REMARKABLE IMAGE PROCESSING

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