Research of Typical Electronic Package Warpage based on GA

Hongwang Zhao [a], Guofu Wang, Yuanhua Chen

Guilin University of Aerospace Technology, Guilin 541004, china

[a]zhw3721@qq.com

Abstract. In order to reduce the warpage value of the electronic package device under the temperature load, improve the reliability of the device. The finite element analysis model of the typical electronic package device was established, and loaded finite element analysis of temperature, obtained the warpage value of the top and middle part of the package structure. 16 different combinations of different parameters were designed by orthogonal design, and the finite element analysis model was established, the corresponding warpage values were obtained and the neural network fitting was carried out. On this basis, the use of genetic algorithm to optimize the material size to achieve the purpose of reducing the amount of warpage. The results showed that the method can greatly reduce the time and ensure accuracy in the package design. And this method provides a new way for the design of the electronic.

1. Introduction

The ever growing electronic package device in the field fo electronic on-board systems led to PCB integration technologies. Packaging technology was one of the key steps in the development of electronic packaging circuit [1]. In the process of electronic packaging, the changing temperature will result in the warpage of the material, the influencing factors include substrate, bonding layer, chip and packaging material. The key to improve the reliability of electronic packaging was to reduce the warpage caused by temperature[2].

Due to the complexity of the model of electronic packaging, the numerical analysis had been used to analyze the warpage caused by temperature in electronic packaging, however, the simplified method was used to distort the electronic packaging model and material. Not only cannot get a more accurate analysis of the law, but also to reduce the temperature of the feasibility of the design method [3].In literature 5, a mathematical model of process parameters and warpage was established by BP neural network, the results show that the prediction accuracy meets the requirements [5].In this paper, the single core packaging structure was taken as an example, Analysis using nonlinear methods on the basis of 3D finite element model. The influence of material size on warpage was studied.

2. Warpage Analysis of Packaging Circuit

2.1 Geometric Model.

The common electronic packaging structure was composed of substrate, bonding layer, and chip and packaging material, as Fig.1. This paper uses a typical size, as Tab.1.
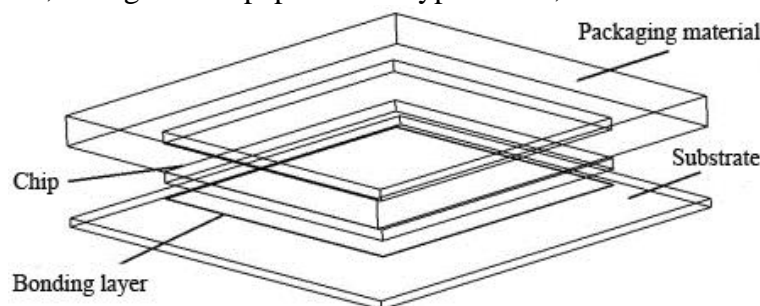

Fig.1 Geometry model of electronic package structure

Tab.1 Typical geometrical dimensions(mm)

	substrate	bonding layer	chip	packaging material
length	10	7	7	10
width	10	7	7	10
height	0.2	0.013	0.254	0.7

2.2 Material Property.

Performance parameters of materials used in electronic packaging circuits were shown in Tab.2.

Tab.2 Material properties

materials	Elastic modulus/GPa	Poisson ratio	Thermal expansion coefficient/10^{-6}℃	T_g/℃
substrate	120.66	0.3	17.2	
bonding layer	See Note 1	0.3	$66(<T_g)$; $290(>T_g)$	-15
chip	130	0.279	2.62	
packaging material	See Note 2	0.3	$7.93(<T_g)$; $20.86(>T_g)$	114.5

Note 1; 2.6GPa(-65℃); 0.17GPa(25℃); 0.08GPa(150℃); 0.12GPa(250℃);

Note 2: 18.706GPa (25℃); 0.653GPa (150℃); 0.588GPa (240℃);

2.3 Finite Element Model

The finite element mesh was shown in Fig.2. Bonding layer was shell element, packaging material, chip and substrate are three-dimensional were solid elements.
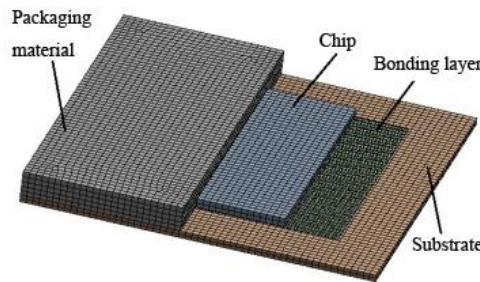

Fig.2 Package structure finite element mesh

2.4 Load and Boundary Conditions

The temperature load of the circuit was reduced to 25℃ of the actual operating temperature from the curing temperature of 175℃.This paper will simulate the real temperature load change.

3. Warpage Results Under Different Sizes

This paper uses four variables,H_1/H_2:the ratio of substrate thickness to chip thickness in electronic packaging structure;S_1/S_2:the ratio of base area to chip area in electronic packaging structure;H_3/H_2:the ratio of packaging material to chip in electronic packaging structure; H_4/H_2:the ratio of bonding layer to chip in electronic packaging structure. According to the actual situation, this paper takes four sets of data for the four variables,H_1/H_2:[0.25, 0.5, 1, 2];S_1/S_2: [1, 1.5, 2, 2.5]; H_3/H_2:[0, 1, 2, 3]; H_4/H_2:[0, 0.05, 0.1, 0.2].

In order to achieve the purpose of the experiment, and reduce the number of experiments, this paper used the orthogonal experimental design method. The method was characterized by simple, convenient calculation table, the user can quickly grasp. When the experiment was arranged according to the orthogonal table, it can not only obtain a very uniform distribution of test points, but also greatly reduce the number of experiments. In this paper, there were four variables, and each variable corresponds to four sets of data, the conventional method required 4^4(256) calculations, this paper selected 4 factors and 4 levels sheet $L_{16}4^4$, Only require to do 16 finite element analysis, as shown in Tab.3.

Tab.3 Orthogonal table finite element analysis data

Geometry parameter				experimental result
H_1/H_2	S_1/S_2	H_3/H_2	H_4/H_2	warpage(mm)
0.25	1	0	0	-0.023
0.25	1.5	1	0.05	-0.038
0.25	2	2	0.1	0.146
0.25	2.5	3	0.2	0.213
0.5	1	2	0.1	-0.018
0.5	1.5	0	0.2	0.073
0.5	2	1	0	-0.034
0.5	2.5	3	0.05	0.115
1	1	2	0.2	-0.012
1	1.5	3	0.1	0.065
1	2	0	0.05	-0.167
1	2.5	1	0	-0.054
2	1	3	0.05	0.012
2	1.5	2	0	0.031
2	2	1	0.2	-0.105
2	2.5	0	0.1	-0.173

4. Warpage Optimization

4.1 Optimization Model Establishment

The reliability of the packaging circuits will be effected by temperature, this paper optimize the geometry of the substrate, bonding layer, chip, packaging material. The goal was to reduce the warpage value by changing the size of the geometry, so as to improve the reliability of electronic packaging circuit, adjust and optimize the geometry of the four materials. In this paper, the optimization algorithm was based on the finite element analysis data using BP neural network for training and learning, Constructed the BP neural network model to replace the objective function, then the optimal solution was obtained by genetic algorithm, Compared with the traditional method, the optimization efficiency was greatly improved, and the optimization effect was improved.

5. BP Neural Network Prediction Warpage Value

BP neural network was based on the understanding of the human brain, A simplified model of human brain biological neural networks, which was based on physical and mathematical methods, and then through information processing. In this paper, the geometric dimensions of four kinds of materials, such as the substrate, the adhesive layer, the chip and the packaging material, are used as the input layer of the BP neural network.

Based on the warpage value of the finite element analysis in Tab.3. Using BP neural network structure 4-6-1, which randomly selected 12 groups of data as training data, the remaining 4 groups of data were used as test data, in order to judge the fitting performance of the trained BP neural network. In this paper, BP neural network program in the MATLAB software to achieve random 4 groups of data error, as shown in Tab.4.

Tab.4 Predictive value and actual value error

the percentage error of BP neural network prediction value and the actual value				the percentage of average error
11.21%	10.03%	12.41%	11.53%	11.29%

Results in Tab.4 that BP neural network fit temperature warping was not very accurate. Commonly used to improve the ability to fit the way: first, increase the number of experiments; second, change the number of hidden nodes. Increasing the number of experiments was the most effective method, but the efficiency was reduced, virtually increased the cost of time. Change the number of hidden

layer nodes only manually change the program, the cost was low. Changing the number of hidden nodes, training BP neural network to get the different errors, as shown in Tab.5.

Tab.5 Prediction error of BP neural networks with different hidden layer nodes

Hidden node	4	5	6	7	8	9	10	11
average error	14.53%	13.03%	11.29%	11.22%	10.96 %	11.36%	12.23%	13.54%

In the BP neural network, more or less hidden layers don't use training accuracy, less will increase prediction error, and the general assembly over fitting, at the same time increase the amount of calculation and time and even affect the error. The average error decreases first and then increases with the increase of the hidden layer nodes, as shown in Tab.5, the average error of the 8 hidden nodes was 10.96%.

BP neural network can be used to predict the warpage value, under the experimental conditions that H_1/H_2, S_1/S_2,H_3/H_2,H_4/H_2 were 1, 1.5, 2, 0.1. The output value of the algorithm was 0.062, the experimental value was 0.055 by finite element analysis, and Percentage error was 12.7%.

5.1 Genetic Algorithm Optimization

On the basis of BP neural network, the material size parameters were used as variables, the output of the neural network was the output of the objective function, run genetic algorithm to find the minimum. The maximum number of iterations, population size, crossover probability and mutation probability were 50, 20, 0.4 and 0.2, respectively. Floating number coding was used to calculate the average fitness value of the best individual as shown in Fig. 3.
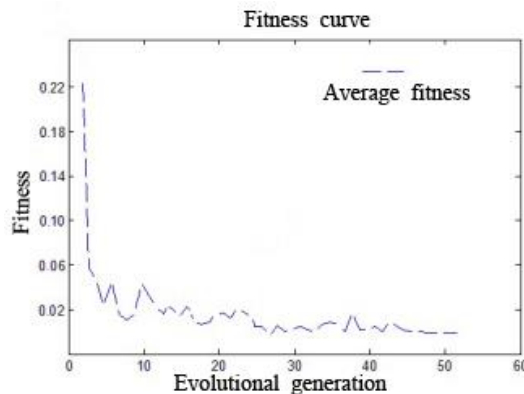

Fig.3 Optimal individual fitness value

The optimal experimental result obtained by genetic algorithm was 0.010, the experimental conditions for the geometric size of materials, H_1/H_2,S_1/S_2,H_3/H_2,H_4/H_2 were 1.6, 1, 2.4, 0.2.the warpage value was less than the experimental data of Table 3, the results show that the genetic algorithm was the best result.

6. Summary

A method presented in this paper provided a new idea for electronic packaging design, which can reduce the design time and cost. It can not only be used to predict the temperature warpage value of the material of the packaging circuit, but also can provide the theoretical method for selecting the geometric size of the material in the initial stage of the package circuit design.

Acknowledgments

References

[1]. Laskar J, Sutono A, Lee C H, et al. Development of integrated 3D radio front-end System-on-Package (SOP)[C]// Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2001. 23rd Annual Technical Digest. IEEE, 2001,p215-218

[2]. Qi L, Du S, Li J, et al. Research on Technology Preventing Warpage Deformation of Large Area PCBAs [J]. Aerospace Manufacturing Technology, 2015,p24-28

[3]. Zhang Weiwei, Zheng Bailin, Zhang Shiyuan, et al.Electronic Package Warpage Simulated with Numerical Method [J].Journal of Tongji University , 2006,34(1),p13-15

[4]. Wang peng, Dai Yun .Optimization Analysis on Warpage Deformation of Electrical Connector Contacts in Injection Molding [J]. Plastics,2014,43(1), p34-38