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An ultrasonic ranging system based on FPGA

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Abstract: FPGA is a high-precision logic device with fast running speed, rich internal resources and reconfigurable strength.This paper puts forward some new ideas for realizing high performance ultrasonic ranging system.This paper investigates the high precision and real-time ultrasonic ranging technology, and designs and completes the design and hardware realization of an ultrasonic system based on FPGA.The system can effectively solve the shortcomings of traditional ultrasonic ranging system in reliability, debugging, real time and measuring accuracy.The system can meet the requirement of the vehicle avoiding, automatic navigation, etc.

1. Introduction

Along with the progress of science and technology, ultrasonic ranging technology has been widely used in all walks of life, especially in the safety warning, automatic navigation and obstacle avoidance vehicles such as areas of non-contact technology requirements.Because of the advantages such as convenience, safety and easy real-time control, the ultrasonic ranging is slowly becoming a mainstream measurement technology.However, in the concrete conditions of the actual work, there are obvious disadvantages to ultrasonic ranging.In today's market, the system is typically based on traditional single-chip computers.Although resource consumption is reduced, there is a great deal of limitation in measuring accuracy and measuring efficiency[1].

2. The system design

In the design of the system, according to the function of the system, there are five main modules.Each is the high-speed counter module, the dual-core FFT module, the time sequence generator module, the echo signal identification module and the waveform generator module.

2.1. The overall framework of system design

The range module USES the hc-sr04 module, the controller USES Altera's Cyclone series FPGA development board, and USES the digital tube as the module to display.The hc-sr04 launch module produces sound waves and is detected by the receiving module when the object is reflected.The FPGA chip will be counted, and the measured distance will be calculated by the digital tube showing the current test results.

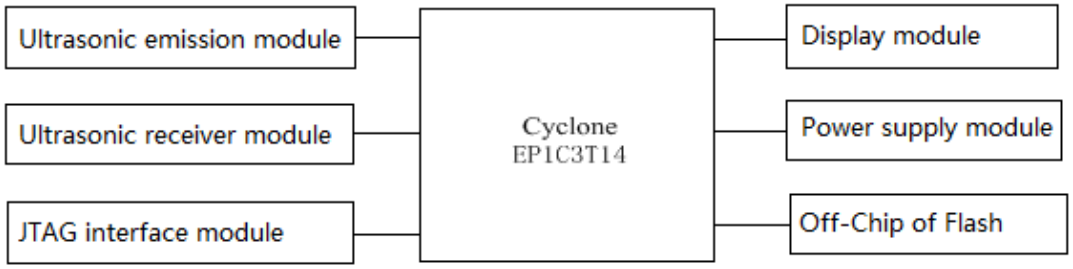

Figure 1 Ultrasonic system structure diagram

In the design of the system, because of the ability to program and debug through the JTAG download line, this is very handy in design.The working process of the whole system as follows, the FPGA development board control clock drive signals and to count at the same time, the ultrasonic drive signal through transmitter, sensor and signal detection, ultrasonic signals emitted by analyte then; Amplifying and enabling the FPGA development board to detect the echo signal through the receiver. Finally, the calculations are shown[2].

2.2. Timing generator module

The effective clock is especially important when designing the sequence generator.This system USES a global clock operation to control timing. In the process of use, the synchronous clock or global clock is a particularly reliable and convenient clock.The global clock is often the first choice for all FPGA design implementations.When used, special clocks are used as input control timing devices. The FPGA development board is dedicated to use as a clock input.

Given that the design USES an external clock to vibrate to a 48-mhz, the subfrequency generates an initial signal of 40KHz as the basis. The frequency splitter is achieved by directly calling the IP kernel of Altera company FPGA.

2.3. Echo identification module

The echo signal recognition module mainly USES the dual-core FFT module to deal with the echo signal, and adopts the design of anti-interference.When the module design is implemented, the logical circuit signal is transformed. When the input signal changes, the output signal does not change at the same time, mainly due to the delay. In this process, the burr signal is produced. This kind of burr signal interferes with the circuit and causes a logical disorder. So, in this process, the solution is to solve the burrs.

A combination of various factors determines the use of locking method to eliminate burrs. The occurrence of the burr is due to the counter output. When the counting bit widens, the variety and quantity of the burrs become more complex. In this case, the output and D triggers are eliminated[3].

In the design of this system, the method of setting the frequency gate valve is used to ensure that the detection is effective and reduce the influence of the interference wave. The function of the threshold valve method is mainly to use the idea of sampling method to determine whether the echo is true based on the measured echo frequency. Assuming that the detection value is smaller than the value of the valve, then the echo signal is identified. Otherwise, ignore it.

The echo signal module is used by the dual-core FFT module to process the signal and use the frequency counting module implementation. In the implementation of the system, the noise of the system itself is not very influential. The ultrasonic receiver is more susceptible to high voltage when

the distance of the distance is slowly changing. The better way to identify the echo signal of ultrasound is the frequency discrimination method. The principle of a specific frequency resolution is to set up a valve signal. That when the design similar to the principle of the frequency divider, is set the global clock signal counts, detection of echo signal value range is within the scope of the valve signal. This implementation mainly USES the three-phase state machine to detect the echo signal.

Figure 2 symbols schematic diagram for echo recognition module, the system clock CLK, rst_n as the reset signal, the echo signal for the receiving end, trig end signal for launch, short [23:0] for calculating the distance display variables.

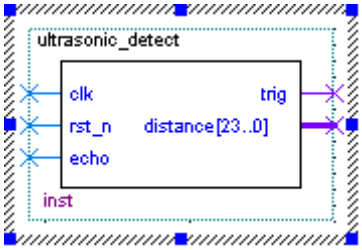

Figure 2 The symbol diagram of the echo signal module

2.4. Dual-core FFT computing module

This module mainly completes the DE2 development board dual-core FFT calculation, which is divided into five main modules by the implementation of the two core FFT modules by the specific requirements of the system. Cordic modules, generator modules, assembly line modules, storage modules, and data conversion modules. As shown in figure 15, the five large modules will also be subdivided to better implement this section. This part of the design is often compared to the FFT implementation. However, the operational control of the data and the flow of data in the design process need to be carefully improved[4]. The two core FFT that is implemented on this basis will meet our requirements.

2.5. Waveform generator module

When designing, the waveform generator module is implemented, mainly on the basis of implementing the sequence generator module. The global clock operates on the frequency division to obtain the drive square wave pulse. After receiving the square wave pulse, the D trigger feature is adopted, and the square wave frequency operation is set up to 50%. And then you get the sensor pulse. This approach can have two benefits: one is to ensure that the driver signal is a square wave of 40KHZ; The second is that the signal can be subdivided and the number of firing pulse counts.

2.6. High speed counter module

The system is designed with a high-speed counter similar to the counter/timer in a single chip. When the FPGA produces a driver signal, the high-speed counter operates. The count stops when the echo signal is transmitted to the high speed counter. In this process, the frequency of counting is known. Finally, the distance of ultrasonic distance is calculated by the method of ranging and ranging.

Counting process, FPGA has the characteristics of running speed and high calculation accuracy, make it easily in the moment to capture the signal echo, so finally the result has the very high precision. After doubling the frequency, the FPGA can be improved. Another advantage is that the FPGA counts more flexible, which can implement any number of counters[5].

The counter USES the counting operation to achieve this method using the count driver signal pulse number. Because there is no command system in the FPGA, this makes the function of the counter primarily designed in the various submodules, and the function of the count by calling each other.

In a stable environment, this property of the speed of the ultrasound, given what we know, is constant. The sound velocity is 340m/s, and ultrasonic sensors are detected. By the principle of ranging, we can calculate the number of single time range pulse counting:

$$N = 2 * \frac{10\text{m}}{340m/s} * \frac{1}{40KHz} = 2353 \quad (1)$$

The N value is 2 and the width is about 12. Thus, the global variable is set to a variable of 20 bits. The following program is for data processing, primarily to convert binary data into actual output data.

```
assign   hundred=distance[8:0]/100
assign   decade=distance[8:0]%100/10
assign   unit=distance[8:0]%10
```

3. System commissioning and test results

In this system, the debugging work mainly revolves around the timing of ultrasonic sensors and the timing of FPGA development board. The core of the whole system is to correctly capture and identify ultrasonic sensor reflections. To make system debugging easier, use the method of online debugging to debug the configuration method of the JTAG download line. First, simple and complicated. Debugging begins with simple logical functions such as frequency, count, etc. The system was designed to be programmed and compiled by the Quartus II 12.0 software. The following sections mainly introduce the system debug method and the test result analysis.

3.1. Embedded logic analyzer

The development of chip manufacturing technology enables FPGA chips to be widely used in a variety of systems, which is also a measure of the complexity of product design. But as the FPGA has become widely available, there have been many problems. Such as: the FPGA's internal signals are difficult to logic analyzer and oscilloscope is detected, the FPGA encapsulation showed a trend of miniaturization and makes noise circuit board itself, etc., these can lead to product validation of the difficulty. For these situations, Altera has developed a dedicated tool, Signaltap II, also known as an embedded logic analyzer. There is a Signaltap II in Quartus. The embedded logic analyzer functions like an embedded oscilloscope and does not take up the I/O port to detect the required signals. Using the analysis and judgment of system performance, the logical analyzer can be removed when the test results conform to the design requirements.

3.2. Module debug waveform

The following diagram is a simulation of high-speed counters, echo recognition, and dual-core FFT modules using logic analyzers.

High-speed counter module debugging

This module by echo, CNT and CLK three synchronous signal is right acquisition and the data flow through the HC - SR04 sensor module to the FPGA, and the data stream processing and then passed on to the next data flow. The high speed counter module waveform is shown in figure 3.

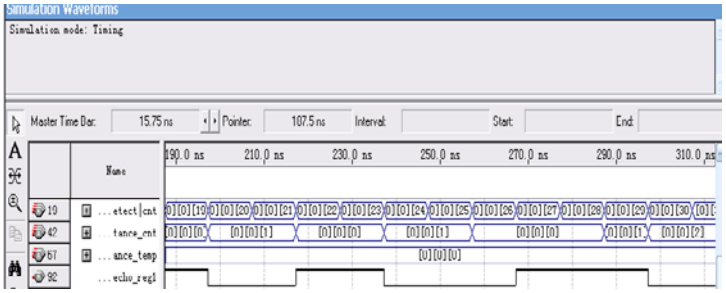

Figure 3 simulation of a high-speed counter

When the system is designed, a filtering operation is performed to filter the redundant signals. The set filtering threshold is 19, which means that the ultrasonic signal is recognized as an ultrasonic signal when there are eight continuous signal pulses. After the system works, the counter will work, and it will always jump between states.

The echo identification module debugging

This module adopts the design of the frequency meter gate valve, and the method of the three-state state machine is used to detect the frequency of real echoes by counting the global clock signal. As shown in figure 4.

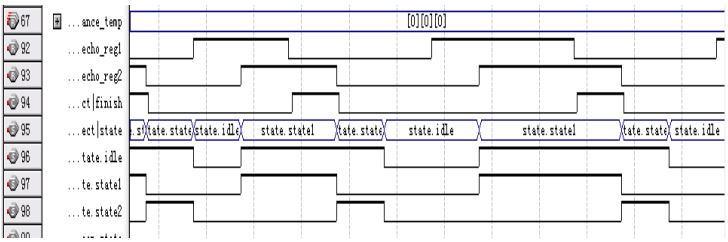

Figure 4 Simulation of echo identification module

When the system is designed, the main function of the echo identification module is to detect the frequency of the echo signal in the set value. Since the echo is emitted by the ultrasound, it sends back the signal, which is needed to detect its validity. As you can see in the diagram, the state signal always goes back to the state_ldle state. This also means that the echo signal detected is not in the threshold, which means that the signal is filtered.

Dual-core FFT module debugging

Figure 5 is the waveform of the dual-core FFT module. As shown, the implementation is the dual core FFT module, which is the FFT operation twice. The result of the counter in address true_addr_a and true_addr_b, will result in high in line_addr_a, low in line_addr_c, transpose line_addr_a line before the address, line_addr_b. The variable qa_data, qb_data is the data that is obtained after passing the module.

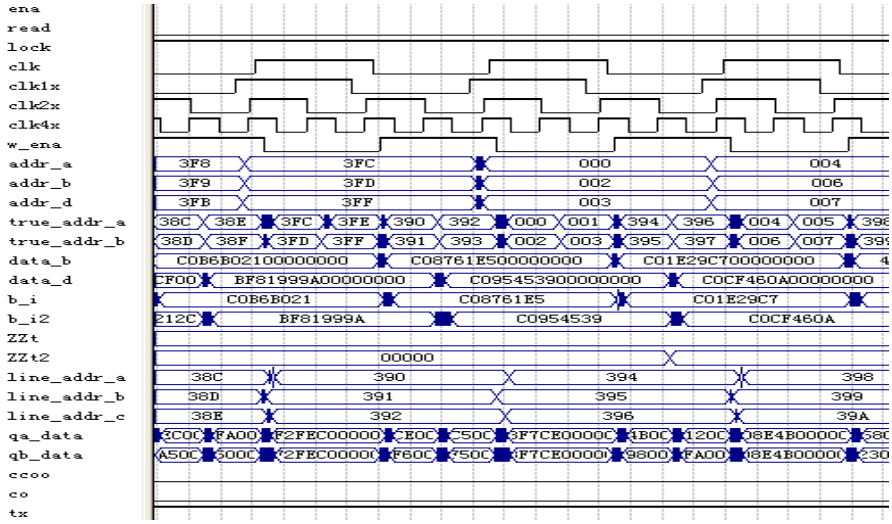

Figure 5 Simulation of the two-core FFT sequence

The entire range system is shown in figure 6. Real-time monitoring is shown by the development board digital tube.

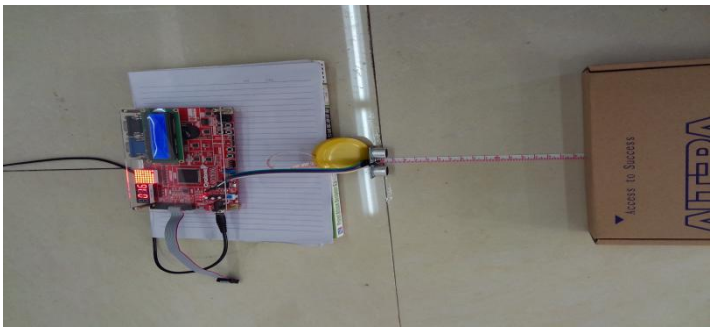

Figure 6 Ultrasonic distance measurement system

3.3. Debugging problems and solutions

The whole system has a lot of problems in debugging. These problems are solved by the debug method implementation. Start by not doing any processing of the ultrasonic signal, which will be collected directly from the original signal and displayed in real time. Is randomly appear garbled words at first, by modifying the CNT count the value of the parameter in the echo recognition module, can see the acquisition of ultrasonic signal, on the digital tube display there is a slight change. It should be a three-phase state machine, the counter signal and the echo detect the result of not synchronization, and then redebug the modules. Modified can be seen in the digital tube ultrasonic distance data real-time acquisition, real-time data on the digital tube, however, shows that the effect is very unstable, change a lot. This big reason is because the frequency meter gate set unreasonable, caused by fixed gate value, set up the most appropriate threshold to detect the effect of echo signal is better. The process of debugging is a tedious and time-consuming process that often requires careful observation and consideration.

3.4. Test results and analysis

The test system are under the environment of the ideal laboratory, the test method is: set up 12 sets of data, for each obstacle measurement data obtained in each group averaged ten times. The details are shown in table 1:

Table 1 Measure data and error

Feet distance measurement/cm	Ultrasonic distance/cm	Absolute error/cm	Relative error/%
200	184	16	8
400	386	19	4.7
600	582	18	3
800	775	25	3.1
1200	1172	28	2.3
1400	1369	31	2.2
1600	1577	23	1.4
1800	1787	13	0.7
2000	1989	11	0.5
2200	2190	13	0.6
2400	2385	15	0.6
2600	2582	18	0.7

As you can see from table 1, the accuracy of the measurement varies with the distance barrier. There are two main reasons for the decline in accuracy; one is too close to the subject; When the distance is too close, affected by the delay of transmitting and receiving circuit, and the system can't timely processing of ultrasonic echo signal, thereby increasing the error. The distance is too large; When the distance is too far, the echo of the ultrasonic wave is weak, and the noise is mixed, which makes a certain effect on the value of the valve. Analysis of the data in the table can be concluded that the near distance obstacle distance in about 20 m, can reach high precision, then the relative error of steady at around 0.5%, can meet the needs of the majority.

When the system is implemented, there are two ways of doing it according to various environmental conditions. One is to increase the frequency of ultrasonic frequencies if accuracy is to be made. But this approach would narrow the range of probes; The second is to increase the detection range and reduce the precision of demand detection.

3.5. Performance analysis of the system

The system has two main advantages:

Control of signal frequency

The typical one-chip microcomputer is 12 megahertz, which normally doesn't exceed 40 megahertz, with a period of 1 to 4us. The operation of the system is in sequential mode, and the method of producing ultrasonic signals is mainly used by the timer interrupt implementation, thus the error of the us level is achieved. However, the sensor required for the system is 40MHz, and each pulse cycle is 25us, which makes it impossible to achieve precise control.

The FPGA is used to divide the clock by the high-speed counter, the clock frequency of the chip is 60MHz, and the program execution runs in parallel. A 40K Hertz division is available through 750, allowing the error to be controlled to nanosecond levels.

Control of signal transmission time

As noted above, the single-chip machine has a range of 1-4us. Using a single chip as a control system, the transmission time is measured using timers and interrupts. The ultrasonic signal is

produced, and the counter works to count. Single-chip machine cycle is 1 us, it is the use of sequential execution, analyte so the farther away, the greater the execution time, the corresponding error will have more.

Since the FPGA is measuring the transmission time by setting up the counter, the clock is controlled by the frequency of the divider, and the uplift is counted to achieve this function. In the counting process, the error can be controlled at the ns level, and the execution of the program USES parallel methods. Therefore, the precise control of transmission time can be achieved.

4. Summary

The main work of this paper is the design and implementation of ultrasonic systems. The system USES a FPGA chip instead of a single chip as the main control chip, to prevent the distortion of the signal and to add FFT modules to the system. This kind of design method solves the common system real time difference, the defect of low accuracy greatly improves the measurement precision of the system.

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