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A Multistage Heuristic Tuning Algorithm for an Analog Silicon Neuron Circuit

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Abstract

This research looks at an ultra-low power subthreshold-operated silicon neuron circuit designed with qualitative neuronal modeling. One technical challenge to future implementation of such circuits is parameter tuning—a problem stemming from temperature sensitivity of subthreshold-operated MOSFETs and the uniqueness of individual circuits in a neuronal network due to transistor variation. This research proposes a fully automated parameter tuning algorithm that combines two heuristic approaches to search for appropriate circuit parameters over a range of temperatures. The algorithm can tune the circuit to behave as a Class I or Class II neuron.

Keywords: neuromorphic engineering, analog VLSI, silicon neurons

1. Introduction

Analog silicon neurons, electronic circuits that mimic the electrophysiological characteristics of neuronal cells, may in the future be used as fundamental building blocks of neuromorphic technologies like brain-mimetic computers. These circuits operate in continuous time, consume low power, and are expected to be implemented in massively parallel networks that are fundamentally different from digital transistor logic circuits[1]. The circuit used in this research is an ultra-low power analog silicon neuron designed with the techniques of qualitative modeling—an approach which seeks to reduce the complexity of ionic conductance models by describing the same dynamics with fewer variables[2]. Such a model allows for replication of a wide variety of spiking dynamics in neuronal cells, including Class I and Class II in Hodgkin's classification[3], with a less complex low power circuit. Power consumption is further reduced by operating the circuit's metal-oxide-semiconductor field-effect transistors (MOSFETs) in their subthreshold regime[4].

The large number of circuit parameter voltages, the temperature sensitivity of subthreshold-operated MOSFETs, and the problem of transistor variation among circuits of equivalent design means that effective parameter tuning to achieve consistent neuron-like dynamics is a significant challenge. A parameter tuning algorithm that addresses these issues will be necessary for future implementation of these circuits in large scale networks.

This research is inspired by positive results in [5] in which the Differential Evolution (DE) algorithm was used to tune the parameter voltages of a conductance-based silicon neuron circuit. The DE algorithm is an evolutionary algorithm which begins with random solution vectors, in this case vectors of circuit parameter voltages, evaluates their performance with a cost function, and passes on elements of vectors with good performance to the next generation[6].

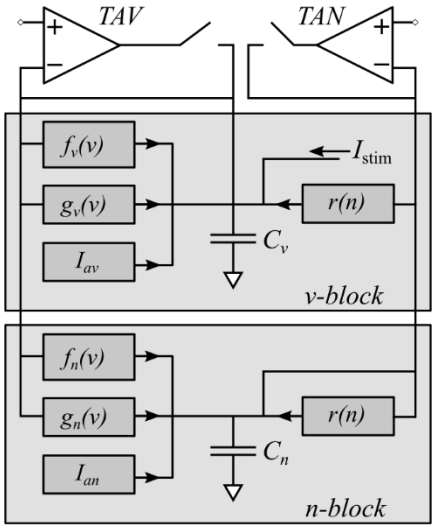

Fig. 1. Block diagram of silicon neuron circuit, reprinted from [7]

In [7], we presented a script which pairs the Spectre circuit simulator with optimization algorithms to automatically search for optimum circuit parameter voltages over a range of temperatures. Two heuristic approaches were used to improve upon a previous trial-and-error based tuning method. In this paper, we present a multistage tuning algorithm which combines those two heuristic methods with consideration given to their merits and drawbacks, and adds an additional pretuning stage to make the algorithm completely automated. Our new algorithm eliminates the need for trial-and-error, only requires input of benchmark characteristics, and can tune the circuit to behave as a Class I or Class II neuron over a range of temperatures.

2. Circuit Description

The silicon neuron circuit is divided into a *v*-block and an *n*-block which each integrate the currents from transconductance circuit components over a capacitor. Variables v and n represent membrane potential and abstracted ionic activity and are coded by subtracting the voltage over their respective capacitors from V_{dd}. The system equations are as follows:

$$C_v \frac{dv}{dt} = f_v(v) - g_v(v) + I_{av} - r(n) + I_{\text{stim}} \quad (1)$$

Table 1. Spectre Circuit Parameters (x=v,n)

Circuit	Spectre Parameter	Function
$f_x(v)$	fx_Vb	scaling
	fx_Vdlt	offset
$g_x(v)$	gx_Vm	scaling
$r(n)$	rn_Vm	scaling
I_{ax}	Iax_Vb	scaling
	Iax_Vin	fine tuning

$$C_n \frac{dn}{dt} = f_n(v) - g_n(v) + I_{an} - r(n) \quad (2)$$

The current-voltage relationships for $f_x(v)$, $g_x(v)$ (x=v,n), and $r(n)$ are sigmoidal curves. A detailed description of these circuits is given in [2]. I_{ax} (x=v,n) are transconductance amplifiers used as constant current sources and I_{stim} is an externally applied stimulus current. Transconductance amplifiers *TAV* and *TAN* use a voltage clamp method to draw the nullclines—curves on which the system equations equal zero—which are used to describe the dynamics of the silicon neuron[8]. All transistors in the silicon neuron circuit are operated in their subthreshold regime, yielding desirable exponential current-voltage characteristics and power consumption as low as 3 nW.

3. Multistage Parameter Tuning Algorithm

Our algorithm requires the user to input the benchmark circuit characteristics: the nullcline structure, circuit behavior detailed in Sec. 3.3, and current-voltage curves of the I_{ax} and $r(n)$ circuits (x=v,n) at 27°C. The user then selects the target temperature that circuit parameter voltages are generated for.

Circuit simulations were conducted in the Cadence software environment with the Spectre circuit simulator on two X5570 processors (2.9 GHz, 8 threads).

3.1. *Stage I: Pretuning*

As listed in Table 1, parameter voltages Iax_Vb and rn_Vm scale the current-voltage characteristics of the I_{ax} and $r(n)$ circuits (x=v,n). The first stage of the algorithm uses Differential Evolution to find the optimum value of these parameters at the target temperature. The cost function is the mean absolute difference of the current-voltage curve resulting from a given parameter to the

current-voltage curve of the circuit with benchmark settings at 27°C.

$$f(x) \triangleq \frac{1}{k}\sum_{i=1}^{k}|I_i(x) - b_i| \quad (3)$$

x is the parameter value for a given simulation; $I_i(x)$ represents each point on the current-voltage curve yielded by a given parameter value; b_i represents each corresponding point on the benchmark curve; and v = 0 V when k = 1 and v = 1 V when k = 101. For each of these three circuits the DE algorithm is used once, requiring about 1.5 minutes and 130 iterations.

3.2. *Stage II: Nullcline tuning*

The second stage of the algorithm uses the DE algorithm to tune the nullclines to match the benchmark nullclines at 27°C in the range of 250–500 mV for Class I and 300–450 mV for Class II. Spectre simulations of the silicon neuron circuit's nullcline mode are run with the input being a vector of circuit parameters. The parameters for Class I are gv_Vm, fx_Vb, and Iax_Vin (x=v,n). The parameters for Class II are gv_Vm, fn_Vb, and Iax_Vin (x=v,n). The roles of these parameters are listed in Table 1. gn_Vm and the scaling factors for the I_{ax} circuits from the pretuning stage are kept constant, and fv_Vb is kept constant in Class II mode. The $r(n)$ circuit is set to zero in the nullcline mode and is not directly evaluated.

The cost function is the magnitude of the vector of the mean absolute differences of the v and n nullclines from their respective benchmark nullclines.

$$g(\mathbf{x}) \triangleq \sqrt{\left(\frac{1}{k}\sum_{i=1}^{k}|v_i(\mathbf{x}) - b_i|\right)^2 + \left(\frac{1}{k}\sum_{i=1}^{k}|n_i(\mathbf{x}) - c_i|\right)^2} \quad (4)$$

$v_i(\mathbf{x})$ and $n_i(\mathbf{x})$ represent the points on the output v and n nullcline curves for parameter settings $\mathbf{x}$; b_i and c_i represent the corresponding points on the benchmark v and n nullclines at 27°C; v = 250 V when k = 1 and v = 500 V when k = 151 for Class I; and v = 300 V when k = 1 and v = 450 V when k = 151 for Class II. Differential Evolution for this stage of the algorithm typically requires 16 thousand nullcline mode simulations and 8 hours of calculation time.

As reported in [7], the DE algorithm accurately replicated the benchmark nullclines at a variety of temperatures, but did not yield accurate transient behavior, suggesting the need for an additional tuning stage.

3.3. *Stage III: Tuning transient behavior*

The final stage of the algorithm uses rn_Vm from Stage I and gv_Vm, fn_Vb, and Iax_Vin (x=v,n) from Stage II as the center of a 5 × 5 search space by adding +/– 0.5 and +/–1 mV to each of these five parameter values. A brute force approach is then used to evaluate each of the 5^5 = 3125 combinations of parameters in this search space by running transient simulations of the circuit. The circuit is then subjected to 5 and 10 pA sustained stimuli and the spiking frequency is evaluated using data from an 800 ms time period.

The cost function evaluates each parameter set by calculating the magnitude of the difference vector between these two simulated circuit behaviors $\mathbf{j}(\mathbf{x})$ and their benchmark values $\mathbf{b}$, a vector calculated from simulation results with a parameter set which yields typical Class I behavior at 27°C.

$$\mathbf{j}(\mathbf{x}) = \begin{bmatrix} 5\text{ pA stimulus response} \\ 10\text{ pA stimulus response} \end{bmatrix}, \qquad \mathbf{b} = \begin{bmatrix} 17.91 \\ 36.87 \end{bmatrix}$$
$$h(\mathbf{x}) \triangleq \|\mathbf{j}(\mathbf{x}) - \mathbf{b}\| \quad (5)$$

Class II neurons are characterized by the sudden onset of periodic spiking when subject to an adequately strong sustained stimulus. The cost function in Class II mode evaluates a vector of the circuit's frequency response to 5, 7.5, 10, and 12.5 pA sustained stimuli. $\mathbf{b}$ again was calculated from simulation results with a parameter set which results in typical Class II behavior at 27°C.

$$\mathbf{j}(\mathbf{x}) = \begin{bmatrix} 5\text{ pA stimulus response} \\ 7.5\text{ pA stimulus response} \\ 10\text{ pA stimulus response} \\ 12.5\text{ pA stimulus response} \end{bmatrix}, \qquad \mathbf{b} = \begin{bmatrix} 0 \\ 22.08 \\ 30.21 \\ 35.3 \end{bmatrix} \quad (6)$$

Stage III concludes with a polishing step which interpolates the optimum parameter set between the elements of the original search space. The entire stage requires about 4 hours of calculation time to run all the transient circuit simulations. Increasing the search space exponentially increases calculation time, thus illustrating the need for nullcline tuning in Stage II.

Table 2. Algorithm results with benchmark behavior highlighted in grey. "X" indicates non-neuron-like behavior and "D" indicates decaying response.

	Temperature (°C)	2	7	12	17	22	27	32	37	42	47
Class I	I_{th}(pA)	X	289.5	248.5	202	164.5	172.0	147.5	145.5	147.0	148.5
	5 pA response (Hz)	X	17.91	17.91	17.91	17.91	17.91	17.91	17.91	17.91	17.91
	10 pA response (Hz)	X	36.87	36.87	36.87	36.87	36.87	36.87	36.87	36.87	36.87
Class II	5 pA response (Hz)	0	0	0	0	0	0	0	0	0	0
	7.5 pA response (Hz)	22.0	D	D	D	D	22.1	22.1	22.1	0	0
	10 pA response (Hz)	29.5	30.3	30.6	30.8	30.6	30.2	30.1	30.2	0	0
	12.5 pA response (Hz)	35.1	35.3	35.4	35.5	35.4	35.3	35.4	35.3	0	0

4. Results

The algorithm was run in Class I and Class II modes for 2° to 47°C in 5° steps and the results are listed in Table 2. For Class I, the circuit displayed behavior closest to the benchmark in the range of 7° to 47°C. 2° did not yield neuron-like behavior. The threshold current I_{th} is the minimum current required for a 500 μs pulse stimulus to generate an action potential. The threshold current ranged from 289.5 to 145.5 pA and descended roughly as temperature increased. Class II does not exhibit threshold-like behavior so this category was not recorded.

In Class II mode, transient behavior nearly identical to the benchmark was observable for 32° and 37°C. At 7°, 12°, and 22°C the 10 pA and 12.5 pA sustained stimuli induced spiking at a similar frequency to the benchmark, but the 7.5 pA response decayed after a few iterations. A simplified version of the algorithm which does not contain the Iax_Vb tuning step in Stage I yielded behavior nearly identical to the benchmark at 22°, suggesting that slight modifications to the algorithm may improve the decaying problem for 7–22°C.

5. Discussion

The multistage heuristic tuning algorithm considers the merits and drawbacks of the DE algorithm-based nullcline tuning and brute force transient tuning approaches as noted in [7] and combines them into a hybrid approach which in simulation can effectively tune the silicon neuron circuit to behave as a Class I or Class II neuron over a range of temperatures. The next step will be to implement a version of this algorithm with the actual silicon neuron circuit using LabVIEW or Python.

This algorithm could also be effective in dealing with issues of transistor variation in a network of silicon neurons, since it can find unique parameter sets which may yield similar nullcline structure among individual members of a network. Future silicon neuron circuits may be designed with on-chip feedback mechanisms which automatically adjust parameter voltages based on the results of a tuning algorithm.

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