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Methodological Research on Low Power Design for Portable Mixed-signal IC

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Abstract. Block diagram of digital part for portable IC is given. Three ways to reduce the power consumption of digital circuit are introduced. Several circuit modules of analog part for the portable IC are listed, and low power design for these modules are described in detail.

1. Introduction

Power efficiency is the most relevant design concern for portable Integrated Circuit. These ICs usually include digital part and analog part in it, and power may be consumed by these two parts correspondingly.

For digital part, it is a fully static CMOS design, and can support the power saving mode for its applications required very low standby current. HALT and STOP low power operation mode can be used, Digital IC offer the power-down function that forces itself enter standby mode to save the power consumption. By selecting reasonable I/O configuration and designing sophisticated memory structure make digital IC be a low-power consumption product series.

For analog part, voltage reference, comparator and oscillator are common circuit modules, and the total power of analog part will be decided by theirs, so low power design for these modules are described in this paper.

2. Low Power Design Technology for Digital Circuits

2.1 Block Diagram

Digital part of an Integrated Circuit usually include Sequential Logic and Combinatorial Logic, then Memory is an important module. In addition to that, I/O Port is often needed in IC. A typical digital circuit diagram is shown in Fig. 1

In order to cut down the power of digital circuit, A register is used, Fig.1 shows the connection relationship between the register and other part of the circuit .The work way for low power of these module will be described in detail in next sections.

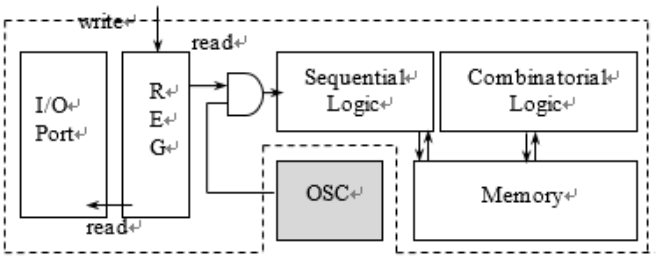

Fig. 1 Digital Circuit block diagram

2.2 HALT and STOP Mode

For power saving, a software controllable standby switch is built-in. First the user can simply enable the wake-up sources , and then stop the main clock by writing the STOP clock register, The circuit will go to standby mode, and the whole chip enter the HALT mode. The HALT mode saves the memory contents and remain I/O's previous states.

If the users have more requirement for this IC(example for non-timepiece products), then can make it enter a STOP mode, this eliminates the power consumption of all modules ,and this mode will

freezes the oscillator, causing all other chip functions to be inoperative, so STOP mode will places the IC in its lowest-power consumption mode.

They are some wake-up sources in IC, for example key wake-up. After the IC is woken up, it will go to the next state of HALT/STOP, and this action will not affect both memory and I/Os.

2.3 I/O Configuration Selecting

IF bi-directional ports are not used in application circuit, They should be set as input mode with pull-low option to save power. For power savings(reduced leakage current), ports are always read as "1" while port control is equal to "1".When key-change wake up is the only wake up source, users should set key wake-up enable system register before entering into sleep to turn off OSC for power saving purpose.

Consider with power consumption about different switches, auto feedback pull-low resistor is applied to reduce current. Fig. 2 shows the I/O structure for low power consumption.

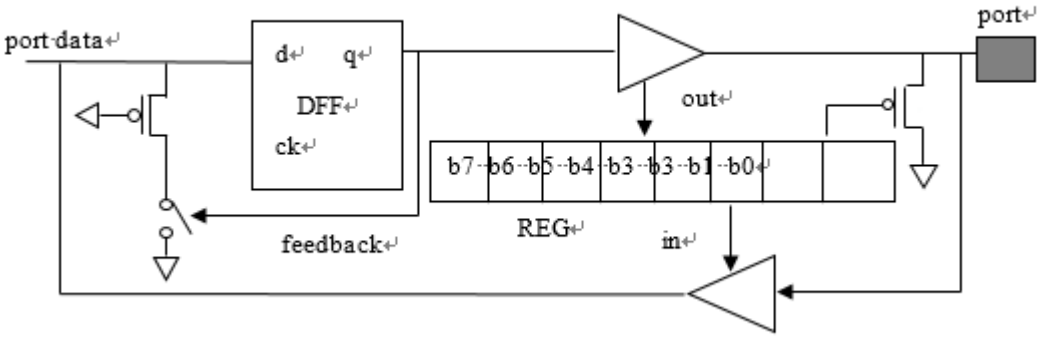

Fig. 2 Low power consumption I/O structure

2.4 Memory Structure Designing

For low frequency ROM, to reduce the chip size, pre-charge structure is adopted. MOS transistor Mp and Mn are controlled by the same signal prechrg, normally named as pre-charge transistor and evaluate transistor. To reduce power consumption, Mn is necessary, If Mn is not existed, when pre-charge is valid("0" level), address for NMOS array should invalid.

3. Low Power Design Technology for Analog Circuits

Voltage Reference, Comparators and Oscillator are three most common circuit structures in analog circuits, the power of these structures may have a very important impact on the total power of analog circuit. Low power design technology for these circuit structures will introduced here.

3.1 Ultra-Low Power Voltage Reference Design

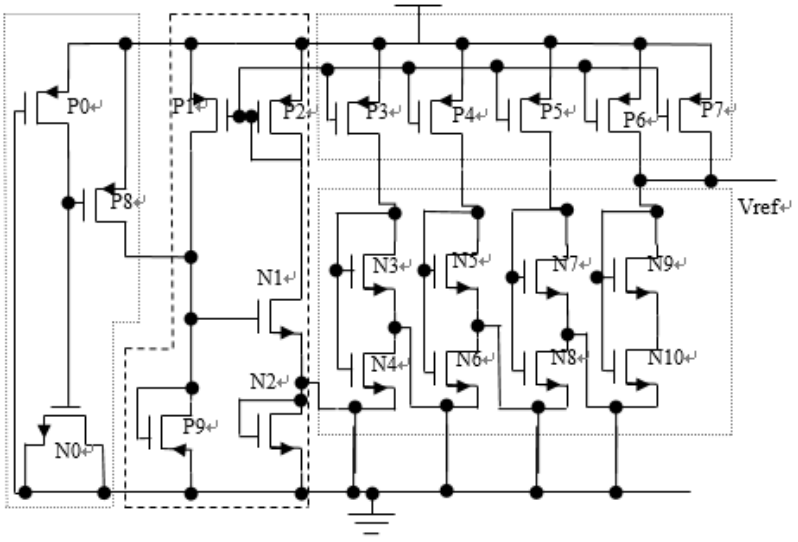

Fig. 3 Voltage Reference circuit presented in this paper

The structure of the ultra-low power voltage reference circuit is shown in Fig.3. The overall circuit consists of four sub-modules. The first is the start circuit. The sub-module consists of three MOS transistors, one of them as a capacitor to reduce the capacitance area. The second sub-module is the current mirror circuit, which consists of seven common gate PMOS, resulting in the same size of the mirror current for other modules. The third sub-module is CTAT circuit which consists of the current mirror circuit and three MOS transistors worked in the sub-threshold, the CAT produces a negative temperature voltage at the drain of the MOS named N2. The last sub-module is the multi-stage PTAT circuit which consists of four pairs of NMOS operating from the self-biased sub-threshold to produce a multi-stage PTAT voltage, this voltage integrate with the CTAT voltage in the output point, and get zero temperature coefficient reference voltage.

As the above-mentioned voltage reference circuits work in the sub- threshold, the overall operating current is only 8nA, thus greatly reducing power consumption. The minimum operating voltage of this voltage reference is only 0.8V.

3.2 The Circuit Structure of Dynamic Comparator

Comparators are often used in analog circuit designs. In a low-power design of analog circuits, a comparator structure called latched amplifier is often used, this amplifier has two stages, and it is a combination of Negative exponential step response of preamplifiers and positive exponential step response of the latch. Through the combination of the two structures, the speed of the comparator is optimized. Fig. 4 is the amplifier latch comparator structure.

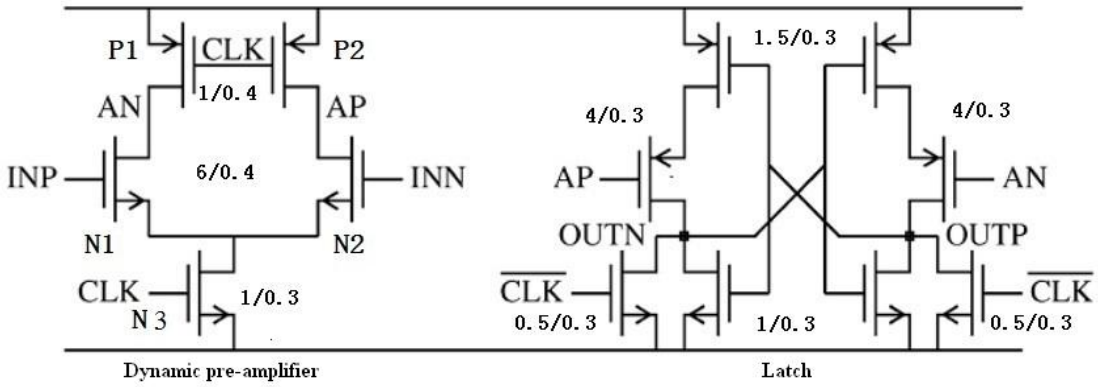

Fig. 4 The structure of Amplifier latch comparator

In Fig.4, the first level is the dynamic pre-amplifier level and the second level is the latch level. The pre-amplifier's trip voltage V_J can be expressed as:

$$V_J = \frac{V_{OH} - V_{OL}}{A_{f0}} = \frac{2A_{f0}\left[1\text{-}e^{-(t_p/RC)}\right]KV_J}{A_{f0}}$$

Where V_{OH}-V_{OL} is the output difference, A_{f0} is the small signal gain at low frequency of preamplifier, t_p is delay time of the amplifier, K is the amplifier stages, R and C is the equivalent output resistance and capacitance of the amplifier.

The latch output voltage difference value (V_{OH}-V_{OL})can be expressed as:

$$V_{OH} - V_{OL} = e^{\frac{t_l}{\tau_l}} \bullet \Delta V_0 = e^{\frac{t_l}{C/g_m}} \bullet \Delta V_0$$

Where t_l is the delay time of the latch, τ_l is time constant of the latch, g_m is the equivalent transconductance of the latch, C is its equivalent output capacitance, $\Delta V0$ is the initial output voltage difference value of the latch.

The whole comparator in Fig.4 is divided into Reset and Regeneration phases. In Reset phase, the Clk is low, and the first stage PMOS pre-charges the node AN or AP to VDD (the PMOS operates in the linear region, the output common mode approaches VDD), the N3 is turned off, So that there is no path to the ground, while the output of the second stage is pulled down to ground by the NMOS which is turned on to achieve the purpose of Reset. In Regeneration phase, the Clk is higher, the N3 is turned on, the AN or AP node starts to discharge, and the discharge speed is different due to the input voltage. The faster will turn on the corresponding second stage input transistor, then the second

stage begin to amplify and regenerate. One output of second stage rise to VDD rapidly by the positive feedback, the other output is pulled down to ground. The overall circuit only consumes power in Regeneration phase, so the power is very small.

3.3 Low Power RC Oscillators Design

This paper introduces an low power RC oscillator, the structure shown in Fig.7,where Y2 is the control signal. When Y2 is high, N5 turns on , P4 turn off, Power supply is divided by R1 and R2 to provide Reference voltage (Vref), the circuit is working properly,otherwise when Y2 is low, the circuit is not work and the oscillator is turned off.

When the capacitor is charging or discharging ,the potential of the two electrodes of the capacitor cannot sudden change, and this is the working principle of RC oscillator. Therefore the cycle of the RC oscillator can be controlled by the voltage at both ends of it.

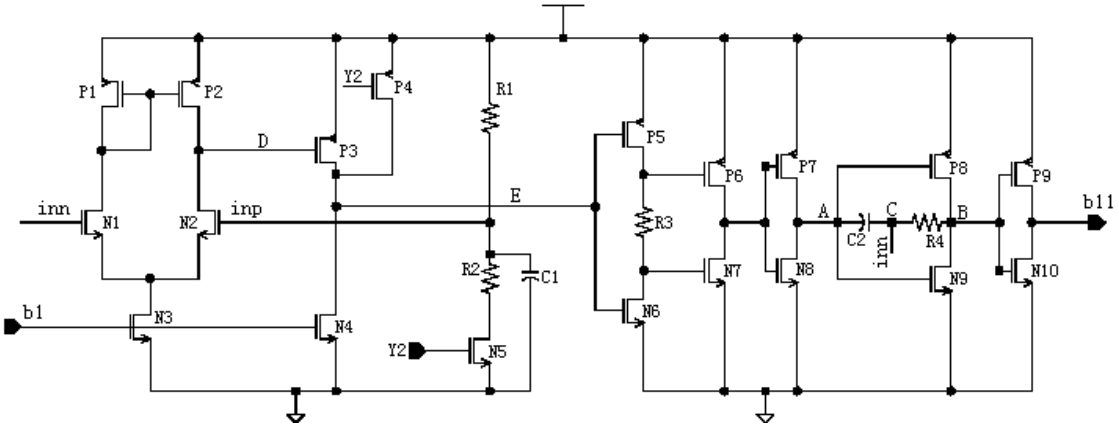

Fig. 5 Low Power, High Precision CMOS RC Oscillator Circuits

For the circuit shown in Fig. 5, the value of Vref can be changed by adjusting the ratio of R1 and R2, thereby the duty cycle of the output square wave can be changed. The main function of the resistor R3 is to reduce power consumption. Ffirst of all, it can limit the current of its own branch, because P5 and N6 are transistors with opposite W/L ratio, and their equivalent resistance is large. The resistance R3 is also great in order to be able to compare with the equivalent resistance of P5 and N6. In addition, under the action of R3, P6 and N7 cannot be turned on at the same time, this resulting in very small power consumption at circuit branch with P6 and N7.

4. Summary

By using both hardware and software solutions, we has designed portable mixed-IC to cover many application fields which required very low standby current. We put these principles into practice, and it shows that they are reasonable and useful.

Acknowledgements

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