Design and Implementation of AMT Boot Subsystem

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Abstract—Automated Mechanical Transmission technology and new energy vehicles is the development direction of the market, gearbox system software application prospects, the foreign relevant departments have taken strict confidentiality measures to gearbox system software design and calibration methods, the domestic is relatively less, the relevant literature is not much. Therefore, the research and design of system software that support the transmission calibration, program updates, parameter update, will promote the development of the domestic automotive industry. The system is divided into working subsystem and boot subsystem based on the stability and security of the system. The boot subsystem is mainly used for updating the program and parameters. The working subsystem is used to realize the normal start and shift. And then proposed interrupt redirection technology and data verification algorithm, while the completion of the guidance subsystem design and implementation. Experimental tests show that the design and implementation of the boot subsystem is correct and effective.

Keywords: Automated Mechanical Transmission, Transmission Control Unit, MC9S12XEP100

I   Introduction

With the development of transmission, the technology of automatic control of transmission has gradually become mature. Many types of automatic transmission, according to the current implementation of the different ways can be divided into the following four: Hydraulic automatic transmission (AT), Automated Mechanical Transmission (AMT), Continuously Variable Transmission, (CVT), Dual-clutch automatic transmission (DCT) [1].AMT on the basis of the traditional gear mechanical transmission to the Transmission Control Unit (TCU) as the core, the use of electronic technology and automation control theory, through the hydraulic, pneumatic or motor drive actuator to complete the vehicle's automatic shift, automatic start and other functions [2]. Transmission system software technology is one of the key technologies in automatic transmission design, so research and design of low cost, perfect function, high reliability AMT system software will promote the development of automotive speed technology.

In order to improve the development efficiency of AMT, the system needs to support the program download and parameter update, taking into account the

security, in the design need to increase the boot subsystem. The guidance subsystem integrates the calibration device function and can upload the parameter data to the calibration device in real time. When using the calibration device to control the AMT, the system can be updated, the parameters updated. The design of the boot subsystem improves the development efficiency and safety performance of AMT products.

This article uses NXP's MC9S12XEP100 as the core processor of TCU. To ensure system security, the system is divided into two subsystems: the boot subsystem and the working subsystem, and the two subsystems perform different functions. The working subsystem is the normal working procedure of the gearbox, and the guidance subsystem is used for program downloading, calibration parameter update and transmission box information inquiry and update. This paper mainly completes the design and implementation of the guidance subsystem, and does not study the working subsystem in detail.

II   Interrupt redirection technique

The system should support the downloading of the program and the updating of the parameters. Considering the security of the system, the system cannot be in the normal working state when downloading the update. Therefore, the guidance state outside the working state is designed. The boot state is realized by the boot subsystem. Because both the boot program and the working program use the interrupt handling mechanism, there are situations where the same interrupt source is used but different processing is done. Therefore, a way to implement a mechanism for implementing different operations using the same interrupt source must be designed. Through the analysis of the processor operating mechanism, designed two sets of programs.

Option 1 is to apply for a space in memory INT_BUF, used to store the address of the interrupt handling function, in the boot state, mount the boot system interrupt service function. In the working state, mount the working system interrupt service function. The design passed the test, but this program there is a drawback, is to guide the subsystem, for each interrupt function to establish a processing function, so as to ensure that the normal

working system interrupt service routine can be a normal response.

Option 2 uses interrupt redirection technology, with interrupt redirection register IVBR in MC9S12XEP100, determine the location of the interrupt vector table. The high address of the interrupt vector index area is set by writing the specified value to the IVBR. For example, if the IVBR default address is 0xff, the address range of the interrupt vector area is 0xFF00-0xFFFF. If the IVBR is set to 0xD0, the interrupt vector address is 0xD000 - D0FF. There is also a drawback to using interrupt redirection, that is, the interrupt vector area of the normal working subsystem is intercepted from the compiled file, the address range is 0xFF00-0xFFFF, and then downloaded to the specified interrupt vector area at download time.

Through analysis and comparison, second schemes are used in the design.

III   Data validation algorithm

In the process of storing the program and parameters, the ECC check algorithm is adopted taking into account the security of the system. Memory is an electronic device, the system in the memory read and write may be an error. Memory access errors mainly include two types: hard and soft errors. Hard errors are caused by damage to the memory, resulting in incorrect data, hardware errors cannot be corrected by algorithm. Soft error is caused by the system in the access memory is due to electronic interference and other factors.

Error Checking and Correcting (ECC) check is to add the check code in memory, through the check code can check or correct the memory error occurred in the data. ECC memory to support the verification, each piece of data storage space will have several corresponding ECC check code storage space. When the system writes to the memory, the ECC check code of the data is generated according to the system support ECC algorithm and the ECC check code is stored in the specified check memory space. When the system reads the memory, the system checks the read data according to the check code, verifies which error in the data, and corrects the error bit, the memory controller passes to the system is the correct data. Using the ECC check method to verify the stored data will reduce the performance of the system, but from a security point of view, this check is necessary.

When an error is detected by ECC check, FECCRIX is used to select the corresponding word in the FECCR register sequence to be read. FECCR register contains the check unit or double bit error results, FECCR register provides access to some ECCRIX defined domain, when the fault information stored in the specified register, only the fault bit is cleared, the other fault information will Was rewritten. The FECCR register can only be read and cannot be written.

When writing to 0x1 on the FECCRIX register when checking for PFlash, the upper 7 bits of the address bus

are fetched by reading the FECCR register. When writing 0x01 to FECCRIX, the lower 16 bits of the address bus are acquired by reading the FECCR register. When writing 0x010 to 0x101 to FECCRIX, it is possible to acquire four words of data and to read the check word when the Pflash block data is incorrect. For D-FLash, the error data address is fetched by writing to the FECCRIX register 0x00, 0x01, and the incorrect 16-bit data is obtained by writing 0x10 to the FECCRIX register.

The system supports ECC interrupts containing double bit failure (DFDI) and unit failure (SFDI) when reading chip data. The system uses the ECC check mode when reading the Flash information. If the interrupt is generated when the data is read, the data is rewritten by checking the address of the wrong data.

When a read operation is made to Flash, the ECC algorithm modifies the error bit if a bit error occurs and reads the restored value instead of the true value when reading and writing Flash. If you want to remove this bit error, you must rewrite the entire 256 bytes of the sector.

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IV   Design and Implementation of Boot Sub–system

A.   The overall design of the boot subsystem

The main task of the boot subsystem is the program download, parameter update and information query function, the use of memory space 0xE000-0xFFFF, where 0xFF00-0xFF for the reset and interrupt vector area. To prevent the bootstrap program from being corrupted, the WP and NE bits of the resolution register cannot be protected by the configuration to 10, which is set to read-only and executable.

After the normal operation of the AMT system, the gearbox will work in the working subsystem. Only after establishing the connection with the calibration device, the calibration device controller will send the boot command to enter the boot subsystem. Under the guidance subsystem, the gearbox is not in the process of data sampling and driving the solenoid valve. At this time, the program download and the parameter are updated and more secure.

After the system starts, according to the startup parameters to enter the boot subsystem, the boot subsystem must first make some of the required hardware device initialization, including the system clock settings, CAN bus communication initialization, Flash initialization. After the completion of these tasks into the idle state, waiting to receive the task of the calibration device, when the calibration device to receive the task, the implementation of the task, after the implementation of the system into the idle state. The system clock settings are shown in Formula 1, 2, 3

(1) $Fvco = 2 * Fosc * (SYNDIV + 1 / (REFDIV + 1)$

(2) $Fpll = Fvco / (2 * POSTDIV)$

(3) Fbus = Fpll / 2

Where Fvco represents the Voltage-controlled oscillator frequency (Hz); Fpll represents the phase-locked loop frequency (Hz); Fbus represents the bus frequency (Hz); SYNDIV, REFDIV, POSDIV the register setting.

The system requires a bus frequency of 24MHz, TCU hardware circuit processor connected to the external crystal is 16MHz. The requirements for installing the system are set as follows: SYNR = 0x2, REFDV = 0x1, POSDIV = 0, CLKSEL = 0x80 (select phase locked loop).

After the system clock is set, you need to set up the CAN communication device. Which CAN equipment to be set to expand the frame, the bus frequency is set to 500K Kbps, and according to the need to set the filter and interrupt priority. Flash initialization main settings bus frequency, EEE programming error handling, ECC check and so on.

B.   Program download design and implementation

MC9S12XEP100 itself supports JTAG and BDM interface download. As the drive has been loaded generally do not set the program update interface, so that the system upgrades to bring trouble. Taking into account the practical application of the system to increase the boot process, in the boot process, the system can support the program updates through the CAN network. To achieve the program download function, the first boot program through the BDM interface programming to the processor, and this area is set to protected mode, to prevent the program to run away from the contents of the boot program. The working subsystem program can be downloaded from the CAN bus to the AMT system. The system supports the maximum download of 256k bytes of the program. In order to prevent the loss of the original program, the system alternately stores the program to the work area 1 and work area 2, so that if the system fails to power down the program programming failure, AMT system can resume the last start of the program.

When updating the working program of the system, it is necessary to ensure the correctness of data transmission and writing to PFlash. In the bus transmission process need to carry out data packet verification. After the code is written to the PFlash memory area, the processor checks the write data for verification. If the write data is not correct, it will be rewritten. If a frame fails to send three consecutive times, it means that the program download fails. The program download state transition procedure is shown in Fig.2.
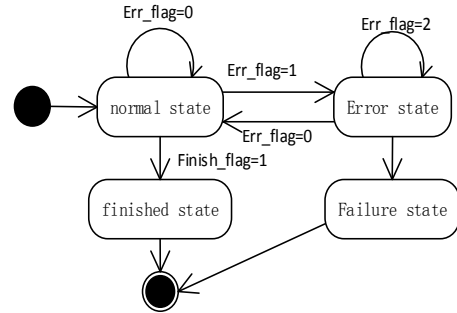

Fig.2 Program download status transition diagram

In order to ensure the correctness of the program download, in the process of downloading the program, the use of ECC checksum. The size of each sector of the system is 1k. When programming a sector of a system, the sector must be erased first. In the program download design, when writing data to the new sector, first apply 1K data buffer, and then erase the specified sector, each received 8 bytes of data to write data to the data buffer The Write data after reading, if not check the fault, then continue to receive data. If an ECC fault occurs, erase the sector, rewrite the data in the data buffer into the specified sector, and check whether the fault has occurred by reading the data in the sector and exit the task if a fault occurs. After all the machine code is written, the TCU writes successful acknowledgment information to the calibration device data, see Fig.3.
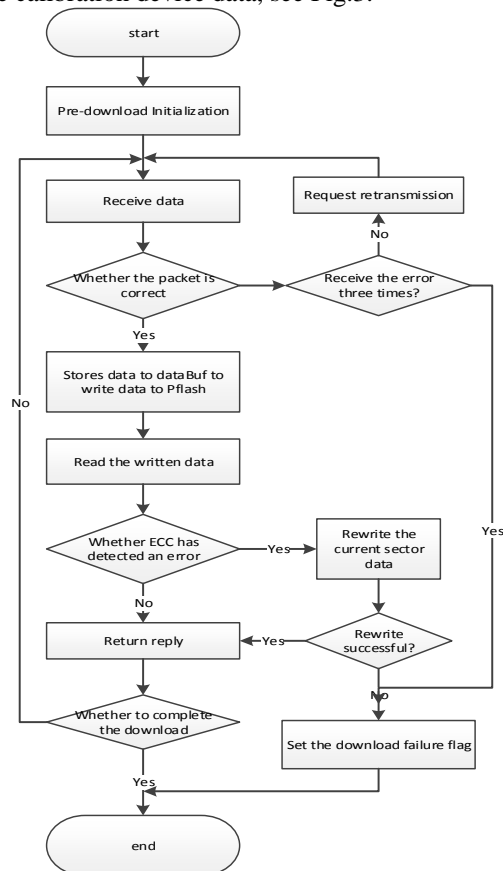

Fig.3 program download operation flow chart

C. Design and Implementation of Parameter Download

The parameters required for the system are stored in page 0 of the variable DFlash. System parameters are divided into three categories: system startup parameters, AMT information parameters, calibration parameters. Storage addresses 0x0000-0x01FF. The system supports the calibration device to update the parameters of the gearbox. The updatable parameters include the gearbox information and control parameters. All parameters of the gearbox are stored on page 0 of the DFlash. Before storing the parameters, the contents of the DFlash area must be erased. DFlash supports the minimum erase unit for the sector, each sector is 256 bytes, and the average use of each parameter space is 2 bytes, so erase will lead to the loss of other data. So in the design, the parameters downloaded before the first RAM in the application of 256 bytes of space. When parameter updating is required, all the contents of the sector where the parameters are located are copied to RAM, then the parameters to be updated are received, and the received data packets are checked. If the verification fails, the parameter update fails. If the verification is successful, the contents of the RAM will be changed according to the specific parameters to be updated. According to the download notification to complete all the parameters of the update, the use of Flash common command (FCCOB) in the DFlash erase, the final parameters will be written to DFlash. After writing is complete, read the parameter information and check for an ECC error. If the contents of the parameters stored in the DFlash are not registered with the ECC error, the write succeeds. Otherwise, the parameter update fails.

D. Design and Implementation of Information Query

The information query includes basic information and control parameter information for reading the transmission, wherein the basic information includes: vehicle type information, transmission information, actuator information, TCU information, sub-transmission information, and software version information. The parameters of the system support query include: selector shift, shift displacement, release selector shift, release shift displacement, clutch control parameters, and so on.

The system receives the query command, the first command to resolve the order to determine whether the command format conforms to the specification, if not meet the specification return command does not have the right to answer, if the query is the basic information, the system directly to the basic information for data encapsulation, After the completion of the package is uploaded to the calibration device. If the control parameter information, because the control parameters designed to the more information, so the use of analytic function by processing the search frame ID and data field informa-

tion to find the index value. Find the address of the DFlash area where the parameter is located based on the index value. Read the data through the FCCOB command, and encapsulate the data into the sending packet and send it to the calibration device.

V Application testing

(1) Program download function of the test

First select the executable file to download, the program will be successful after the download is successful, this time through the calibration device to send to the normal system command, the program can go to the normal system. By querying the current state of the gearbox can query the system has successfully entered the boot subsystem. Through the test, the system achieved the desired requirements.

(2) Parameter download test

The parameter download test contains updates to the basic information and control parameters of the gearbox, by downloading the basic information and control parameters for the gearbox. Through the test, the system has successfully verified the function of parameter updating.

(3) Information query test

The main function of the query function is to query the basic information of the transmission and the control parameters. Through the test, the system of the functional query can be achieved and the query information is accurate.

VI Conclusions

In order to ensure the security of the system, the guidance subsystem of the introduced AMT system and the design of the boot subsystem improve the development efficiency and safety of the AMT product. The design and implementation of the guidance subsystem and the design of the boot subsystem improve the efficiency and safety of the AMT product. But the current system there are still some shortcomings, need to gradually improve in the future design. The current design of the CAN bus through the program to download the function, but not through the CAN bus for online debugging, the problem is the next step in the research work.

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