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Design and Improvement of a Frequency Synthesizer Based on PLL+DDS+PLL

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Abstract

A L-band high performance frequency synthesizer is presented for space TT&C channel. PLL+DDS+PLL structure is used to realize small step-size, high spectrum purity and low phase noise. Experimental result shows that its phase noise is better than -100dBc/Hz@10KHz and its spurious suppression is better than -75dBc. But the additive spurious results co-frequency interference. Find out the case of co-frequency interference and propose corresponding countermeasures by analysis.

1 Introduction

Currently, the basic design method of frequency synthesizer is mainly divided into two categories, namely indirect frequency synthesis based on phase-locked loop (phase - locked loop, PLL) and direct frequency synthesis based on direct digital frequency synthesis (direct digital frequency short, DDS) [1].DDS is a new synthetic technology developed in recent years, with high frequency resolution, short-time conversion, low phase noise, and the defect is that the output signal frequency and bandwidth is limited that restricted to the D/A conversion speed .

Frequency synthesizer is the key component of space TT&C channel, and the high performance frequency synthesizer has direct effect on the performance of the whole system, which is required of low phase noise, small step-size, high spectrum purity and wide-band. To satisfy the above characteristics, frequency synthesizer uses “DDS + PLL” integrated design generally. On the one hand, it can overcome the defects of spectrum purity and output bandwidth of DDS, on the other hand, it can solve the problem of low resolution and the slow conversion speed of PLL [2].

Commonly, space TT&C channel mixes for many times in frequency multiplication to realize frequency conversion, and the local oscillator is provided by frequency synthesizer for mixing signals. So the spurious signal of frequency synthesizer will be brought in the channel inevitably. Space TT&C channel requires high in receiving sensitivity, which reaches -139dBm and even higher. When the spurious signal overlaps the useful signal in spectrum, it will generate Co-Channel Interference, resulting in equipment working abnormally[3].

2 Design

2.1 Technical indicators

In a certain project, it is need to design a L-band frequency synthesizer. The main technical indicators are as follows:

A) Reference frequency: 10MHz
B) Reference phase noise: ≤-150dBc/Hz@10kHz or less
C) Output frequency: 1350MHz to 1450MHz, step 1 KHz
D) Output amplitude: ≥2dBm
E) Phase noise: ≤-100dBc/Hz@10kHz
F) Spurious suppression: ≥70dBc

2.2 Design scheme selection

In the project demand, there is a high requirement of phase noise and spurious suppression. On the market with the spectrum of common module, phase noise can only achieve-90dBc/Hz@10kHz, spurious suppression is only 60dBc. So the project needs to find another reasonable design scheme. At present, there are following three kinds of scheme to design the frequency synthesizer: DDS driving PLL phase-locked synthesis, DDS and PLL frequency mixing, DDS interpolating PLL frequency synthesis. On the basis of the above designs, through the combination, a variety of designs can be derived, to achieve the goal of complementing each other. Through calculation and analysis, we adopt PLL + DDS + PLL scheme, the block diagram is shown in figure 1. The reason to choose this one is that the stray distribution of DDS output can be adjusted by adjusting the DDS clock, which can get higher spectrum purity.

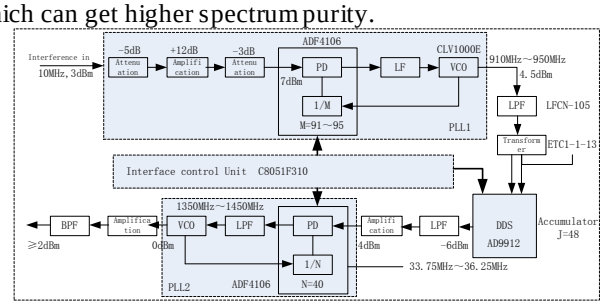


Fig.1 Block Diagram of the L-band frequency synthesizer

In figure 1, the phase-locked loop PLL1 outputs the clock signal that DDS needed, and the clock signal frequency ranges from 910MHz to 950MHz. DDS responding interface control the frequency tuning word of the circuit, and output the signal between 33.75MHz and 36.25MHz. Phase-locked loop PLL2 implements the frequency doubling for 40 times, and final outputs the actual needs of L-band signal.
According to the figure 1, the output frequency:

$$f_{out} = \frac{M * N * K * f_{in}}{2^J} \quad (1)$$

In formula (1), "M" is the time of PLL1 multiplying the frequency; "N" is the time of PLL1 multiplying the frequency; "K" is the frequency tuning word of DDS; "J" is the digit of phase accumulator in DDS; "fin" is the input reference frequency (10MHz).

2.3 The composition and basic working principle of the DDS chip

DDS chip consists of phase accumulator, sine lookup table ROM, digital analog converter and low pass filter[5]. There is much digital amplitude information of sine wave Stored in the sine lookup table ROM. The output frequency of DDS depends on the system reference clock and frequency control word. When setting up DDS frequency control word and reference clock and the output frequency is fixed, the phase increment is a constant determined by the frequency control word, whenever a reference signal of the clock cycle comes, The number of the phase accumulator will be carried out in accordance with the frequency control word accumulation, its output is seen as sine lookup table address, the address represents the digital information of output frequency, then it will convert the information into voltage or current through the D/A converter, and finally outputs the sine waveform by smoothing filter.

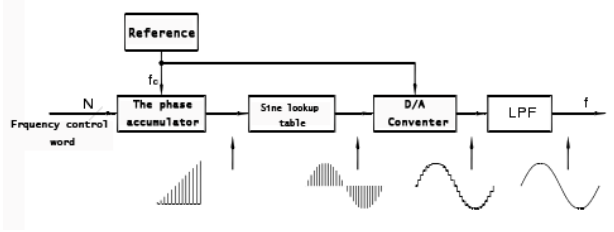


Fig.2 Block Diagram of DDS

2.4 The analysis of feasibility

Output frequency and stepping. The requirement of output frequency range is from 1350MHz to 1450MHz, stepping 1 KHz. This design adopts the "PLL-DDS-PLL" scheme, and the last stage of PLL accomplish 40 times frequency doubling. The clock frequency of DDS is between 910MHz and 950MHz, and it can output the frequency between 33.75MHz and 36.25MHz. DDS uses the AD9912 chip that produced by ADI company in 2007, it has the phase accumulator of 48 bits, when the clock frequency is 1 GHZ, the frequency resolution can reach 44μHz. DDS can get 25Hz stepping easily.

Stray analysis. This project requires that final output stray should be less than 70dBc, so the DDS output spurious suppression[4] is:

$$\frac{S}{N} = 70 + 20\lg 40 = 102(dBc) \quad (2)$$

The proximal stray of DDS mainly include: The ROM amplitude quantization error, the phase truncation error and the DAC conversion error, distal stray is mainly because of the spurious harmonics caused by DAC conversion error. Because DDS output frequency ranges from 33.75MHz to 33.75MHz, less than 1/25 of the clock frequency, so the distal low-pass filter is easy to meet the requirements of remote spurious suppression. In the design, DDS uses the AD9912 chip that produced by ADI company in 2007. The register to control frequency of this device has 48 bits, and the phase accumulator uses 17 bits in addressing ROM and integrates the DAC converter of 14 bits. Otherwise, the device adopts the double channel "spurkiller" technology, which can promote the performance for 10db in spurious suppression.
The stray introduced by ROM amplitude quantization error:

$$\frac{S}{N} = 1.76 + 6.02m + 10\lg\frac{2^k}{4} \quad (3)$$

In the formula, m=14, k=17, so the spurious suppression introduced by ROM amplitude quantization error is 149.1dBc.
The stray introduced by phase truncation error:

$$\frac{S}{N} \approx 6.02k \quad (4)$$

So the spurious suppression is 102.34dBc.
Considering the above two factors, the proximal spurious suppression of DDS can achieve 102dBc, so the spurious suppression of the final output is better than 70dBc.
Phase noise analysis. In this scheme, we uses ADF4106 from ADI company as PLL chip, according to the parameter table, the normalized noise is -219dBc/Hz@10KHz. The phase distinguishing frequency of PLL2 is the same as the output frequency of DDS, and the frequency division ratio is 40. So the phase noise that PLL2 can reach is as follow:

$$\begin{aligned} PN_{PLL} &= -219 + 10\lg f_d + 20\lg N \\ &= -219 + 10\lg(36.25\times10^6) \\ &\quad +20\lg 40 \\ &= -111.4(dBc/Hz) \end{aligned} \quad (5)$$

The result meets the demand of -100dBc/Hz@10kHz. In addition, we can conclude the least phase noise of DDS output:

$$\begin{aligned} PN_{DDS} &= -100 - 20\lg N \\ &= -100 - 20\lg 40 \\ &= -132(dBc/Hz) \end{aligned} \quad (6)$$

According to the parameter table of AD9912, we know the phase noise is better than -140dBc/Hz@10kHz when output frequency is 50MHz. The phase noise of Reference source is not less than -150dBc/Hz@10kHz, which meet the requirement of reference source from DDS output.

Through all the above analysis of the whole system, the index of phase noise can be achieved in theory.

2.5 Product and the measure results

Through the above scheme analysis, combined with the specific design, processing, debugging, and testing, the size of the final product is 160mm×90mm×25mm, and the material object is shown in figure 3.

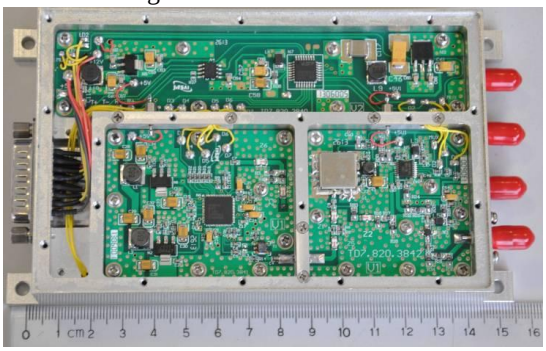
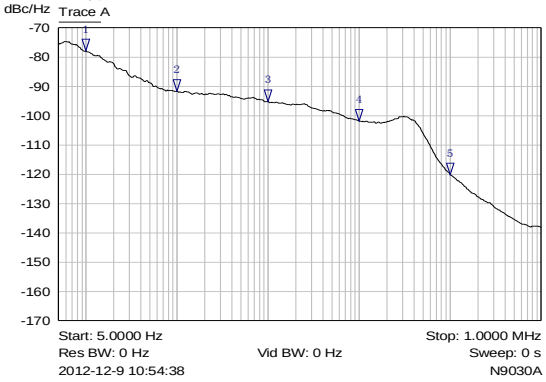


Fig.3 Photo of the L-band frequency synthesizer

We test the synthesizer at room temperature with AgilentN9030A spectrometer, and the SSB phase noise curve is shown in figure 4. The test frequency is 1450MHz, and the power supply is DC 12V and 5V, the measured phase noise reaches -101.7dBc/Hz@10kHz, and the spurious suppression is -75dBc. In power consumption, the group of +12V power needs only 0.07A current, this group of +5V power needs only 0.15A current, the total power consumption is less than 2W. All the indexes are better than the requirements. In 0℃ ～+45℃ , there's only 0.5dB fluctuations I n output, and the rest of the indicators remain unchanged basically.



Mkr	Trace	X-Axis	Value
1 ▽	Trace A	10.0000 Hz	-77.91 dBc/Hz
2 ▽	Trace A	100.0000 Hz	-91.71 dBc/Hz
3 ▽	Trace A	1.0000 kHz	-95.17 dBc/Hz
4 ▽	Trace A	10.0000 kHz	-101.72 dBc/Hz
5 ▽	Trace A	100.0000 kHz	-120.08 dBc/Hz

Fig.4 Measure curve of 1450MHz Phase noise plot

3 Improvement

When used actually, the L-band frequency synthesizer provides the local oscillator signal for the superheterodyne receiver. We find there are useless harmonics signals of 24 times and 25 times from fDDS in the output signal, the amplitude is about -110dBm. The harmonic signals are in the system frequency (840MHz ～ 860MHz).Due to the high sensitivity of the system which reached -139dBm, the co-channel interference is caused.

Table 1 The relationship between output frequency and inner setting before adjustment

Output [MHz]	Division ratio[N]	DDS signal [MHz]	DDS harmonic signal 1 [MHz]	DDS harmonic signal 2 [MHz]
1350～1450	40	33.75～36.25	810～870（24times）	843.75～906.25（25times）

For example, when the synthesizer output frequency is 1360MHz:

$$f_{DDS} = 1360 \div 40 = 34 \quad (7)$$

$$f' = 34 \times 25 = 850 \quad (8)$$

By adding high-pass filter and band-pass on the outgoing end of frequency synthesizer, we can solve the problems. But it costs more, and the solution needs some other matching circuits. In the actual improvement scheme, we changed the frequency dividing ratio "N" and the frequency of fDDS, so the harmonic signal is out of the medium frequency range. The advantage of this method is only making some change in the frequency division ratio and the frequency of fDDS, there is no change in the hardware.

4 Conclusions

The article designed a L-band Frequency Synthesizer Based on the "PLL+DDS+PLL" technology, and the module is excellent in performance with low power consumption, small size, reliable work, and it has already been used in a number of space TT&C systems. The DDS and PLL chip are all mature devices, that in good performance and have low prices. The prominent advantage of PLL + DDS + PLL is that the clock frequency of DDS is variable, and it can consider both the DDS output spectrum and the spurious suppression. The disadvantages of this technology is that the frequency switching will cost a long time (because using two phase-locked loop), and the harmonic component of DDS has not been eliminated thoroughly (it is moved out of the working frequency). But the frequency synthesizer in space TT&C system for switching is not high, and the frequency band is not very wide, so the above two defects are affordable. The design has a certain reference value for the development of frequency synthesizer in the areas such as communication, electronic countermeasure.

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