Research on Application of Embedded System Based on Neural Network in Analog Circuit Fault Diagnosis

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Abstract. With the rapid development of modern electronic technology, the circuit is highly integrated and large-scale, which leads to the complexity of circuit fault diagnosis. Based on this, a method put forward in this paper is to use BP neural network to diagnose the fault of analog circuits. According to the characteristics of neural network embedded system, a hard fault diagnosis system is designed and simulated. The simulation results show that the fault tolerance of analog circuits can be well recognized when the fault tolerance is about 5%.

Introduction

The diagnosis of analog circuits has always been a hot topic, but also a bottleneck problem[1]. So, it is an important research topic to find the most reasonable way. Then, the idea is feasible to diagnose the fault of analog circuit in the research of fault diagnosis method .

The method of using artificial neural network to diagnose analog circuits is very advanced. Since the value of the analog circuit element is not much satisfactory, the loss parameter value of its component tend to be volatile. Then, the parameter value has continuity. The continuity of the parameter values leads to the variability of the circuit state. therefore ,it is not possible to list all the circuit states. The traditional diagnostic method has such a huge amount of computation that it is difficult to operate. In the contrary, artificial neural network is a nonlinear function relationship between the measurement parameter and the fault location, which is fitted by computer. After building the input and output relations with the operation of the sample, fault diagnosis begins. The neural network has strong adaptability, which is very suitable for diagnosing the faults of analog circuits, such as fuzziness, nonlinearity and state variation.

In this paper, the design of embedded system, based on BP neural network technology, is used to study the real time fault diagnosis of analog circuits. The feasibility of the BP neural network technology is verified by the simulation experiment of the embedded system fault diagnosis, which provides guidance for the hard fault diagnosis of analog circuits.

The Theory of Neural Network and Analog Circuit Fault Diagnosis

The Theory of BP Neural Network. At present, BP neural network is one of the widely used methods, with the characteristics of mature theory and stable convergence results and so on[3]. Artificial neural network is to simulate the human brain recognition system for analysis. Specifically, artificial neural network analyze the nonlinear fitting function by simulating the function of real neurons.

The standard BP model consists of three neuronal levels, as shown in Figure 1, there are L processing units in the input layer, M processing units in the middle of the hidden layer, N processing units in the output layer.
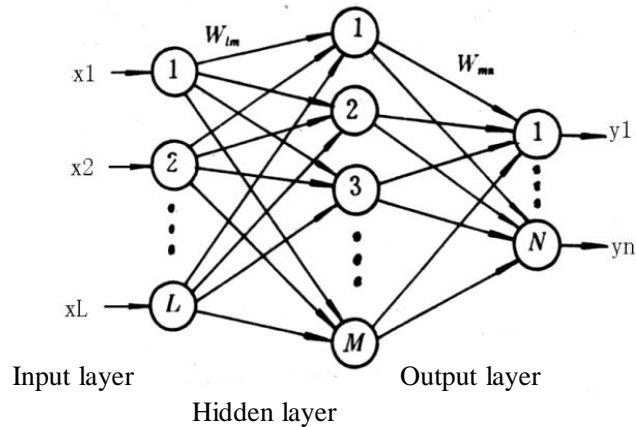
Figure 1　Three - layer BP neural network

　　The BP network performs information processing according to the working principle of the sensor:

$$y(t) = f\left[\sum_{i=1}^{n} W_i(t)x_i - \theta\right]$$

In the formula, $y(t)$ is the time t output, x_i is a component of the input vector, $W_i(t)$ is the weight of the i-th input at time t, θ is the threshold, $f[*]$ is a function.

The following is the perceptron learning rules.

$$W_i(t + 1) = W_i(t) + \eta[d - y(t)]x_i$$

In the formula , x is the learning rate $(0 < \eta < 1)$, D is the desired output (also known as the teacher signal), X is the output of the perceptron.

By constantly adjusting the weight of the sensor, so that $W_i(i = 1, \cdots, n)$ remains unchanged for all samples, the learning process is over

The Theory of Analog Circuit Fault Diagnosis. Generally, analog circuit failure is made up of hard fault and soft fault. This Paper involved the hard fault diagnosis method, which explore the location based on　embedded system about BP neural network.

In order to facilitate the use of neural networks in the computer for fault identification, fault state uses binary representation. Binary representation is used to represent the fault state of 0 and 1, there are mainly two ways to express: N in the expression of the 1 and the normal representation of the coding method. Because of a fault-tolerant performance, we choose the first with to denote the fault condition in this paper. The state of the electronic component is about 0 and 1, respectively, indicating a fault and no fault state. The design of the fault in two ways: the use of OC components in the open circuit fault, SC said the components in a short circuit state. For the two types of hard fault, and the open circuit and short circuit fault of the components, the voltage of the measuring points can be extracted.

Design of Neural Network Embedded System

The Overall Design of the Embedded System. The theory that embedded system distinguishes circuit fault working like this. Firstly, after the transmission of information about the fault circuit into BP network chip through A / D conversion, measurement information then go into the nonlinear function. The result whether the fault circuit is faulty finally displays on the LED screen. So we can realize the fault circuit identification. As we can see, The embedded system is composed

of PC off-line training module, A/D conversion module, data analysis and result display module. The specific module structure is shown in Fig. 2 below.

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                                    ┌──────────────────────┐
                                    │  PC offline training │
                                    └──────────┬───────────┘
                                               ↓
┌────────────────────┐   ┌──────────────┐  ┌──────────────────┐  ┌────────────────────┐
│ Fault detection    │ → │ A/D          │ →│ BP network chip  │ →│ LED display failure│
│ circuit            │   │ conversion   │  │                  │  │                    │
└────────────────────┘   └──────────────┘  └──────────────────┘  └────────────────────┘
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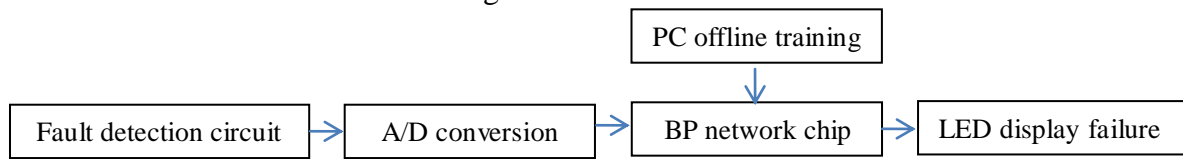
Figure 2.   Embedded System Detection Block Diagram

The key to the fault diagnosis of embedded system based on neural network is to construct a stable and accurate nonlinear function relationship. A large number of data points are obtained by the circuit simulation analysis, and the fault dictionary is constructed. Then the neural network is trained by PC [2]. Through a large number of simulation data, the weights of the BP neural network are stable [5]. And then the stability of the weight is entered into the BP network chip, thus building a nonlinear function of the relationship. Through the analysis of the measured data, the data processing results displayed on the LED screen, so as to make intuitive judgments.

Because the BP neural network not only contains many layers but also has more weight. Moreover, single-precision floating-point value takes more bytes. So, this article uses STM32F103RBT6 chip as a BP network chip. STM32F103RBT6 chip has characteristics, such as 128KB FLASH, 20KB 12, 2 bit ADC, 51 I/O pin configuration, and so on. This will meet the requirements of chip in embedded system well.

Design of BP Neural Network. Generally divided into input layer, output layer, hidden layer, BP neural network will be more stable. The value is very important involving the number of nodes in the three layer, weight, convergence threshold.

The number of nodes in the input and output layer is determined by the number of input and output parameters. In this paper, the fault diagnosis of analog circuit in three kinds of state, namely short circuit, open circuit and normal, is studied. Therefore, it is determined that the number of nodes in the output layer is three, the input layer is controlled by two voltage values, and the number of nodes in the hidden layer is taken as 8.

The activation function of the hidden layer and the output layer uses the Sigmoid function. Relatively, the output pulse threshold is limited to (0,1) or (-1,1). The weights of BP neural networks are solved by iterative method. The empirical value of the initial weight is usually between (-2.4 / F, 2.4 / F) or (-3 / F, 3 / F), where F is the number of corresponding input nodes. The convergence limit is set, once for each iteration, the weights are corrected once until the weights meet the requirements of the convergence limit[4].

Analog Circuit Fault Diagnosis Simulation Experiment and Data Analysis

Based on the design of the embedded system in part 2, this section carries on the experiment simulation analysis. It is designed with 10 electronic components of the pure resistance circuit diagram, as is shown in Fig. 3 below.
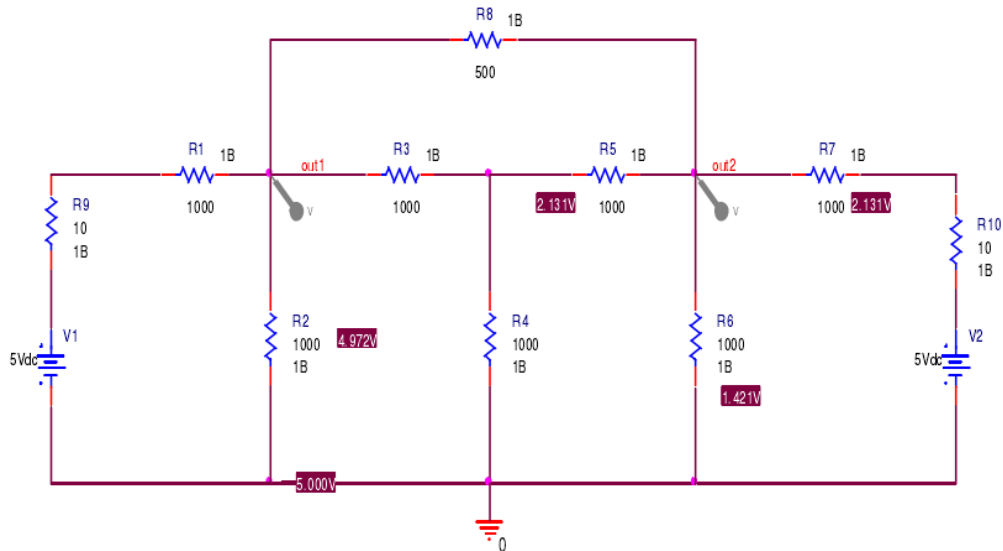
Figure 3. Pure resistance linear circuit diagram

The design of Fault circuit conditions are R1, R3, R4, R5, R6, R7 for the short circuit, R2 for the open circuit. After the design of the embedded system detection, the calculation results are normalized, the results are shown in Table 1 below.

Table 1   Pure resistance circuit fault detection results

V/v		Fault code	status
1	2		
0. 4321	0. 4321	000	normal
0. 9923	0. 714	001	R1 short circuit
0. 5893	0. 521	010	R2 open circuit
0. 3801	0. 419	011	R3 short circuit
0. 3322	0. 3322	100	R4 short circuit
0. 427	0. 3791	101	R5 short circuit
0. 2131	0	110	R6 short circuit
0. 715	0. 9815	111	R7 short circuit

From the above analysis, the correct rate of neural network test is different under different tolerance. In order to further analyze the correlation between the tolerance and the correctness of the test, Monte Carlo algorithm is used to obtain 1000 data sets test. Through testing and analyzing the data, we get the test results under different resistance and tolerance, The correctness of the results is shown in Table 2 below.

Table 2   The correctness of the test results corresponding to different resistance tolerance

Resistance tolerance/%	Correct rate/%
30	21
20	31
10	43
8	56
5	92

As can be seen from Table 2, there is an inverse correlation between the resistance tolerance and the correct rate. The smaller the resistance tolerance , the higher the accuracy of the network test results. The accuracy of the test results is the highest when the resistance tolerance is 5%, and the actual resistance tolerance value is about 5%, which ensures the correctness of the test results of the

embedded system. Therefore, the method of analog circuit fault diagnosis based on BP neural network embedded system is feasible.

Conclusion

BP neural network algorithm has the advantages of faster convergence speed and high accuracy of fault location recognition. In this paper, the embedded system based on BP neural network is designed, the fault diagnosis of analog circuit is realized by BP chip, which can effectively solve the problem of analog circuit fault. It provides a new experience for the realization of analog circuit fault diagnosis.

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