

## Design of MicroBlaze-based Reconfigurable Filter

Wenjie Zhang<sup>1,a\*</sup>, Jinfeng Li<sup>2,b</sup> and Shuilong Zou<sup>3,c</sup>

<sup>1,2,3</sup>Nanchang Institute of Science and Technology, Nanchang, China

<sup>a</sup>568740355@qq.com, <sup>b</sup>524892454@qq.com, <sup>c</sup>1310079831@qq.com

**Keyword:** MicroBlaze; PlanAhead; Restructure; Wave filter

**Abstract.** This paper implements the reconstruction of two filters based on MicroBlaze, the top-level design defines two reconfiguration regions, each of which has four reconfiguration modules, and two reconfiguration regions: All pass, band stop, low pass and high pass, Various configurations of filters are finally verified on the XUPV5-LX110T development board

### Introduction

With the rapid development of semiconductor science, material science, electronic engineering and computer science, The limited hardware resources are becoming more and more inadequate to meet the needs of people, How to achieve more functions on the limited hardware resources has become the direction of people's exploration, Xilinx FPGA (Field Programmable Gate Array) Part of the refactoring has been around for many years. The first part of the JBits and XC6200 series FPGA reconfiguration, but then part of the reconfiguration ability is very limited, the application is very cumbersome and inconvenient. Modular design was introduced in the 2005, but the process was complex, the process tools did not contain software, and the silicon chips were still very limited, so there was a need for more stable, mainstream solutions[1], Current refactoring techniques use the advanced refactoring tool, PlanAhead, Partitions, The process is simpler and easier for users to use. At present, reconfigurable computing has developed a lot. The main goal is to meet the requirements of computing tasks through hardware programming, so as to achieve the best performance. The reconfigurable computing(Reconfigurable Computing, RC) of FPGA is divided into dynamic system reconfiguration and static system reconfiguration.

### Design and Implementation

#### Filter reconstruction top level design

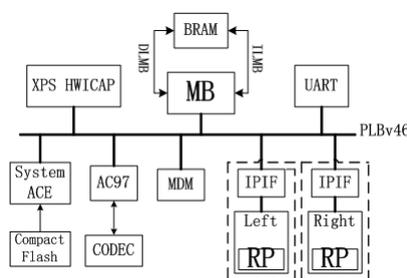


Figure 1. filter reconstruction design

As we can see from Fig. 1, the control core used in the design of the filter reconstruction is MB (MicroBlaze) Embedded soft core, It controls and manages all operations in the filter reconfiguration[4]. The transmission core of the system is PLB (Processor Local Bus) v46 Bus. All peripheral devices, UART (Universal Asynchronous Receiver /Transmitter)、HWICAP (HardWare Internal Configuration Access Port)、System ACE (Advanced Configuration Environment)、BRAM

(Block Random Access Memory)、MDM (MicroBlaze Debug Module)、AC97 (Audio Codec) Are connected directly or indirectly to this bus. The reconfiguration designed in this paper consists of two reconfiguration RP (Reconfigurable Partition) , Each reconfiguration is divided into four reconfiguration modules RM (Reconfigurable Module) : Full pass, band stop, low pass and high pass. Each filter can generate different configurations, and then generate global and partial bit stream. Table 1 lists the main modules of the filter reconstruction system.

Table 1 the main modules of the filter reconstruction system

Name	Describe
MB	MicroBlaze embedded soft core
RP	Reconfiguration partition
CF (CompactFlash)	CF card
AC97	Sound card standard interface
CODEC (Code & Decode)	Audio codec
MDM	Debug module
BRAM	Internal storage
System ACE	System ACE controller
UART	Universal asynchronous receiving and transmitting device
HWICAP	Hardware internal configuration channel port

The modules listed in Table 1 are the main modules of the filter reconstruction system. Among them, the peripheral HWICAP implements the reconfiguration of the dynamic module, and the RP constitutes the two sound channel of the system (left, right) , The ear and the right ear are listening respectively, and the ear can conveniently identify the characteristics of the passband and stopband, and then the correctness of the reconstruction can be judged. AC97 as a standard sound card, after receiving CODEC module processing stereo has its corresponding interface in the FPGA development board, used to plug the headset sound transmission equipment. After the system generates a bit stream download to the CF card, the system configuration ACE configuration in System environment, can be transmitted through the bit stream information[5]. The user uses the super terminal through the UART port to verify the correctness of the system performance.

**Performance Analysis of Filter.** Sound filter used in filter design is embedded in several frequency tone filters in stereo sound stream. It is the function of a specific frequency or eliminate a specific frequency, so that the useful signal without attenuation by as much as possible, so that unwanted signals as large as possible attenuation filter reconstruction needs here there are four kinds: full, with resistance, high and low pass.

**Band Stop Filter.** Bandstop filter refers to through most of the frequency components, but the frequency range attenuation filter to some very low level, and the relative concept of bandpass filter. Bandstop filter can not be directly obtained, it needs the input voltage is applied simultaneously to the low-pass filter and high pass filter, and then the two output voltage circuit the sum, we can get bandstop filter[6]. The cutoff frequency of the low-pass filter should be less than the cutoff frequency of the high pass filter. Fig.2 describes the condition of the band stop filter to filter the sound frequency

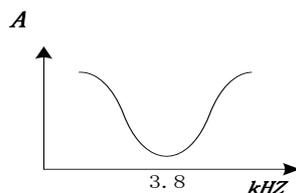


Figure 2. description of band stop filter

**Highpass filter.** The high pass filter function is to remove unwanted low frequency components in the signal. The high pass filter can make the medium and high frequency signal by the low-frequency signal attenuation, and its role is to filter the low frequency components of the audio signal, enhance the midrange and treble components to drive the speaker midrange and high tone unit [7]. in addition, often high pass filter and low pass filter pairs, regardless of which one is to sound a certain frequency to should go to the unit. Fig.3 is a simple description of the sound frequency of filters.

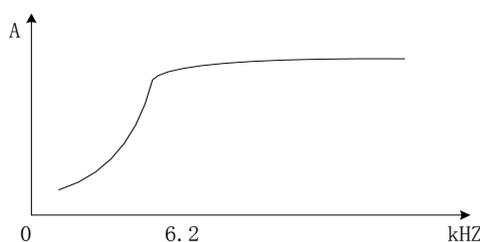


Figure 3. high pass filter description

Can be seen in Fig.3, the sound signal sound frequency is greater than 6.2kHz by filter output, and less than 6.2kHz of the basic sound signals are removed by high pass filter. Through the speaker and the sound signal is filtered out, the human ear can clearly feel the high sound signal than many sharp sound signals all pass.

**Low Pass Filter.** Low pass filter with a cut-off frequency, the frequency dividing signal filter allows the signal below the cutoff frequency can be not affected by, and higher than the cut-off frequency of the signal is attenuated and can not pass through it. The sound signal by the speaker came later, the human ear is feeling deep, no strident voice, and high pass filter principle instead of [8]. low pass filters in a sharp noise environment when used with noise elimination function. Fig.4 depicts the simple low-pass filters the sound frequency.

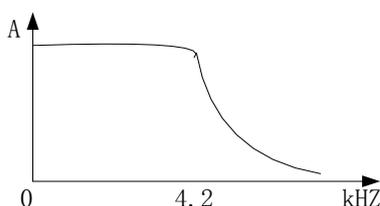


Figure 4. low pass filter description

You can see from Fig.4, lower than the frequency of the voice signal can be output through the 4.2kHz filter, which is higher than the frequency of the voice signal 4.2kHz is not output. After the low-pass filter and the sound signal is spread through the speaker, the human ear can obviously distinguish a sound signal, no noise and sharp.

**Control and Configuration of FPGA.** The hardware system of the processor is built by the Platform Studio work platform of Xilinx Corporation. After that, it is necessary to generate netlist, and then call the netlist in PlanAhead to reconfigure[9].The processor system control and management center is a soft core embedded processor MicroBlaze (MB), it has the advantages of high running speed, less resource, highly configurable, can work together to complete the design of system on programmable chip and other peripheral IP core, widely used in communications, military, and other areas of high-end consumer market. MicroBlaze processor using RISC (Reduced Instruction Set Computer) instruction set architecture and Harvard memory architecture, instruction, data bus width is 32. Three and five lines of MicroBlaze instruction execution: when using the area optimization, the pipeline is divided into three levels, namely the fetch, decode and execute, which can reduce the hardware cost; when do not use the area of optimization, the pipeline is divided into five levels: fetch, decode, execute, memory access and write back, so that it can improve the performance. The MicroBlaze version used in this article is 4, and its instruction is executed as 3 level pipelined mode[10].

**Reconfiguration and Zone Partitioning.** Re allocation and regional division is a key part of filter reconstruction. Has produced all the required netlist file through the EDK tool in the design of hardware system. Here is the system design with PlanAhead: the definition of re allocation (RP), increase the weight of configuration module (RM), the definition of re configuration of regional division operation produce a variety of configuration tools, and generate the whole and part of the bit stream.The definition of re configuration partition is a very important link of reconfiguration, it should be based on each reconfiguration module number and type of resources used to determine [7]. in the design of the reconfigurable module only SLICE can be used. The two division of the general area for reconfiguration: SLICE\_X0Y120: SLICE\_X47Y159.

**Test**

After bit files and configuration files to CF card reader to download through the CF card read, insert the memory card into the corresponding position of the development board, the power to open the development board and super terminal, implement configuration. Fig.5 is the filter test results.

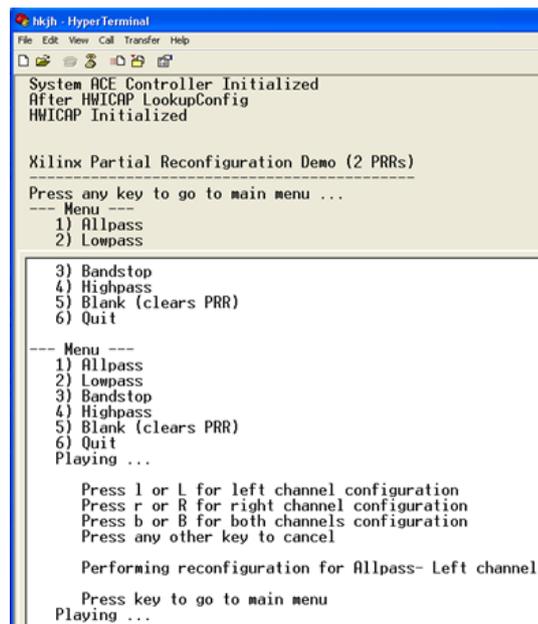


Figure 5. Test result diagram

## Conclusion

This paper is based on the MicroBlaze core, the overall structure of the use of XPS platform to build the hardware system, generate the corresponding netlist, and design a variety of configuration in the PlanAhead tools, which realizes the reconstruction design of the two filters, the final XUPV5-LX110T development board on the Xilinx implementation, has been verified in the super terminal. Reconstruction techniques used in this paper is relatively advanced, but the reconstruction filters are some basic sound filter, to improve the practicality of this design, should do more improvements in filter design.

## Acknowledgements

This paper is funded by sub subject of research project of science and technology of Jiangxi provincial education department in 2016. The original subject number is: GJJ161225. Sub project number is: GJKJ-16-18.

## References

- [1] Wen Yao Xu. Design of self reconfigurable system based on new FPGA .Zhejiang University. Circuits and systems. 2013, 5
- [2] W.M.Fathelbab, M.Steer. A reconfigurable bandpass filter for RF/microwave multifunctional systems. IEEE Trans, Microwave Theory Tech. vol.53, no.3, part 2, pp. 1111-1116, Mar. 2005.
- [3] P.Blondy, C.Palego, M.Houssini, A.Pothier, A.Crunteanu. RFMEMS reconfigurable filters on low loss substrates for flexible front ends. In Proc. Asia-Pacific Microwave Conf. 2007(APMC 2007). Dec. 11-14,2014,pp.1-3.
- [4] M.R.AI Mutairi, A.F.Sheta, M.A. AIKanhah. A novel reconfigurable dual-mode microstrip meander loop filter. In Proc. 38th European Microwave Conf.2008, Oct. 27-31, 2015, pp.51-54.
- [5] Wayne Wolf. FPGA-Based System Design. Prentice Hall Professional Technical Reference, 2014: 5-13.
- [6] Zhao Feng, Ma Diming, Sun Wei, Liang Tianyi. Example of embedded system design on FPGA. Xi'an Electronic and Science University press. Xi'an. 2016.4: 49-133.
- [7] Cai Hongbo, Cai Qixian, Huang Xiaolu, Cai Qizhong. Design and research of a dynamic reconfigurable IP system. A small microcomputer system. Vol.28 No.5 2013.5.
- [8] S. W. Nabi, C. C. Wells, and W. Vanderbauwhede. Towards a Dynamically Reconfigurable SoC for Wireless MACs in Consumer Handheld Devices. In First International Conference on Computer. Control and Communication, pages 182–191, Nov. 12–13, 2015.
- [9] T. Pionteck, L. D. Kabulepa, C. Schlachta, and M. Glesner. Reconfiguration requirements for high speed wireless communication systems. In Field-Programmable Technology(FPT), 2003. Proceedings. 2003 IEEE International Conference on, pages 118–125, Dec. 15–17, 2003.
- [10] T. Tuan, S.-F. Li, and J. Rabaey. Reconfigurable platform design for wireless protocol processors. In Acoustics, Speech, and Signal Processing, 2001. Proceedings. (ICASSP '01). 2001 IEEE International Conference on, volume 2, pages 893 – 896, Salt Lake City, UT, May 7–11, 2001.