ATLANTIS PRESS

Advances in Intelligent Systems Research (AISR), volume 145

2017 International Conference on Electronic Industry and Automation (EIA 2017)

Design of a Voltage Reference based on Subthreshold MOSFETS

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***Abstract*—This article proposed that an ultra-low power voltage reference under low supply voltage took advantage of characteristics of MOSFETS operating in the subthreshold region to meet the low power design. The circuit was designed using 0.18μm CMOS process of SMIC, and simulated after layout using SPECTRE simulation tool. The results showed that good linearity can be attained in a supply voltage range of 0.9-3.0V and the output reference voltage is 600.8±0.65mV. In condition of 1.8V power supply, typical temperature coefficient is 15ppm/℃ between 25℃ and 115℃. Meanwhile under the same condition, the power consumption is only 0.54μW at room temperature. This work can be applied to smart sensor and wearable medical equipment etc, which need low voltage and low power dissipation.**

Keywords-voltage reference; subthreshold region; low power; low voltage; temperature coefficient

I. INTRODUCTION

Voltage reference circuit is generally applied for analog, mixed-signal circuit and system on chip (SOC) in microelectronics. The purpose of designing voltage reference is to achieve a relatively stable output reference voltage which is independent of temperature and insensitive of supply voltage [1]. Traditional bandgap reference voltage resource generating an output voltage about 1.2 V limits the range of the supply voltage [2, 3]. With the development of IC technology, an increasing number of literatures and research groups focus on the design of the low voltage and low power circuits.

The design approached that MOSFETS should be designed in the subthreshold region where devices also have electronic characters of transistors under the lower gate-source voltage. In [2], the circuit utilizing transistors operated in the subthreshold region still adopted traditional bandgap voltage reference configuration was at the expense of precision and chip area. Based on the same region, [4] proposed a new configuration circuit with good performance, but the topology is complicated that directly reflecting in the chip area. In [5], although the new configuration circuit utilized transistors operated in the subthreshold region, the requirement of ultra-low power was not good satisfied. The problem exists that MOSFETS do not operate steadily due to CMOS process variation [6, 7]. However, traditional bandgap voltage reference is not adaptive for the production, e.g., wireless sensor networks, self-powered devices, energy harvesting circuits and implantable medical devices of ultra-low power [8]. To solve these problems, under the precondition of the reliability of the chip, we have to consider designing a new kind of ultra-low power voltage reference.

Based on the above, a new voltage reference that can operate in nano-ampere and with low supply voltage is proposed in this article. Based on the subthreshold region, the gate-source voltage of a single NMOS possesses a negative temperature coefficient (TC) [7], and the output voltage of two series connection NMOS possesses a positive TC. So we could assume that the voltage reference with zero TC can be obtained by adding the two signals. On account that the consumption is almost from obtaining reference voltage with a zero TC, the circuit could achieve the objective of low supply voltage and low power dissipation.

II. CIRCUIT CONFIGURATIONS

Figure 1 shows the entire voltage reference circuit we proposed. The circuit consists of a start-up circuit, a current source subcircuit and a bias voltage subcircuit. The marked NMOS (NM1-NM8) are operated in the subthreshold region, and PMOS are operated in the saturation region. The current source provides a mirror current with zero TC and at the same time it is solid which means that with high PSRR and independence on process variation. The bias voltage subcircuit consists of two series connection pairs NMOS (NM1, NM4 and NM3, NM5) and a transistor NM2 which formed a coupled loop. So the circuit obtained a constant voltage by combining two voltages with a positive TC and a negative TC. The following sections describe the principle in detail.

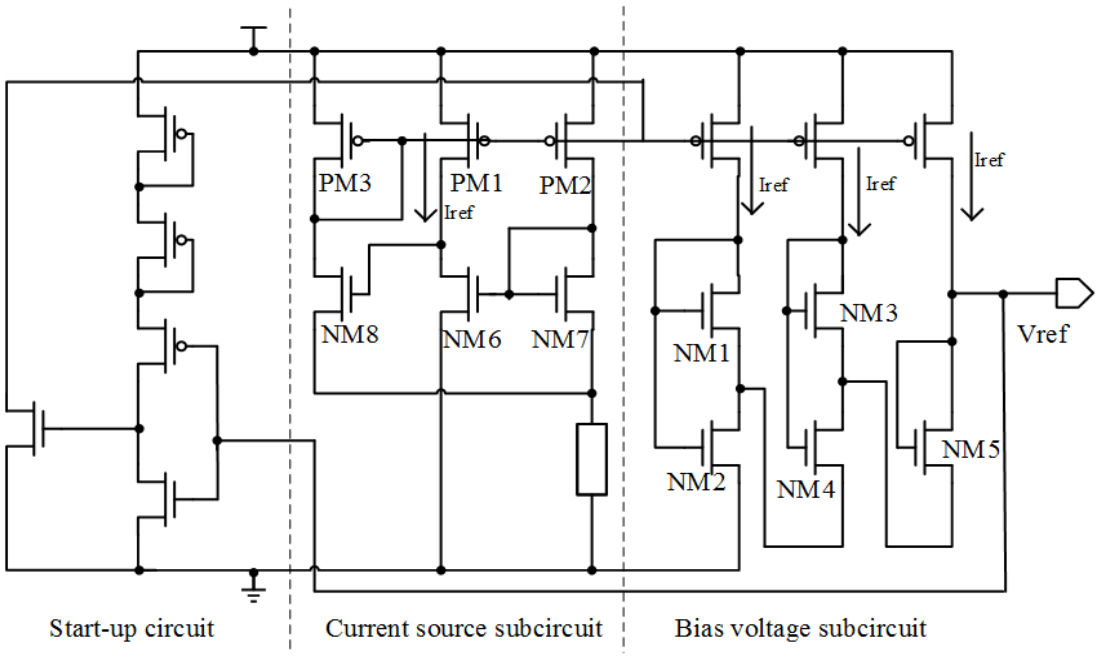

Figure1. Entire circuit of the voltage reference which is based on the subthreshold region

A. *Temperature Dependence of Current Source Subcircuit*

Current reference is one of the important module blocks for analog circuit, and it has a direct influence on performance of entire circuit e.g. power dissipation, PSRR and TC. Based on the subthreshold region, through predicting subthreshold model we can obtain a constant output current.

The subthreshold drain current I_D of a NMOS is an exponential function of the gate-source voltage V_{GS} and the drain-source voltage V_{DS}. The expression is as follows

$$I_D = \frac{W}{L} I_0 \exp\left(\frac{V_{GS}}{\xi V_T}\right) * \left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right]. \quad (1)$$

$$I_0 = \mu C_{ox}(\xi - 1)V_T^2. \quad (2)$$

$$\mu = \mu_0\left(\frac{T}{T_0}\right)^{-m}. \quad 1 \le m \le 2 \quad (3)$$

Where I_0 is the unit saturation current, $V_T (= kT/q)$ is the thermal voltage, $\xi (>1)$ is the subthreshold slop factor [9]. For $V_{DS} > 200mV$, current I_D is independent of V_{DS} and the expression is

$$I_D = \frac{W}{L} I_0 \exp\left(\frac{V_{GS}}{\xi V_T}\right). \quad (4)$$

We assumed that the aspect ratio of NM6, NM7 is $\frac{W}{L}$, and the multiplier of NM7 is K_7, so the output reference current is given by

$$Iref = \frac{W}{L} I_0 \exp\left(\frac{V_{GS6}}{\xi V_T}\right) = K_7 \frac{W}{L} I_0 \exp\left(\frac{V_{GS7}}{\xi V_T}\right). \quad (5)$$

Therefore,

$$Iref = \frac{\xi V_T \ln K_7}{R}. \quad (6)$$

While MOSFET is operated in the subthreshold region, the movement of charge carrier chiefly is diffusion therefore the carrier mobility can be ignored. At present the TC of the output reference current is related to the resistor and the aspect ratio of the transistors.

We can obtain higher PSRR by using three branch current source. It is because of the negative feedback of the third branch in current source subcircuit. Consideration about the negative feedback loop when supply voltage works, the lifted drain voltage of NM8 leads to small current, so that the voltage difference of the resistor becomes smaller and this devotes to lower drain voltage of NM8, eventually we obtained a solid current. Otherwise we can use smaller resistor by increasing the current of the third branch circuit.

The typical value of current based on the subthreshold region is usually under μA. And we estimated a 30nA output current source as pre-design plan. Firstly make a prediction of the aspect ratio of the transistors. The multiplier of NM7 is usually even number for the sake of layout, and equation (4) shows that we'd better to choose small number for small current. We assume that the multiplier of PM3 which copy the current through PMOS

mirror current is K, and compromise K is 4 for larger branch current to get small resistor.

Rewrite equation (6), the third branch current is given by

$$I = \frac{\xi V_T}{R}\frac{1}{K}\ln K_7. \quad (7)$$

For zero TC current, the TC of resistor meets

$$\frac{\partial R}{\partial T} = \frac{\partial V_T}{\partial T} * \frac{\xi}{I} * \frac{1}{K} * \ln K_7. \quad (8)$$

Where K is the multiplier number of PM3, K_7 is the multiplier number of NM7. There is a positive correlation between the thermal voltage and temperature, i.e. $\partial V_T / \partial T > 0$, so, to obtain zero TC current need positive TC resistor for compensation. Usually we choose two resistors of opposite TC to achieve zero TC reference current.

B. Dependence of Output Voltage on Temperature

The bias voltage subcircuit achieve temperature compensation through combining two series connection pairs NMOS (NM1, NM4 and NM3, NM5) and a transistor NM2. The gate-source voltage of NM2 operated in the subthreshold region has a negative TC, and is given by

$$\frac{\partial V_{GS}}{\partial T} = \frac{\partial V_{TH}}{\partial T} + \xi\frac{k}{q}\ln(\frac{I_{DS}L}{\xi I_0 W}). \quad (9)$$

Where threshold voltage is given by $V_{TH} = V_{TH0} - \kappa T$, and has negative TC. The value of the subthreshold slope factor ξ ($=1+\frac{C_{dep}}{C_{ox}}$) is between 1 and 2. So the gate-source voltage of NM2 has a negative TC by adjusting the aspect ratio of the transistor, and is given by

$$V_{GS}(T) = A - BT \text{ [10]} \quad A>0 \quad B>0 \quad (10)$$

So we can conclude that the gate-source of a single NMOS has a negative TC and we can utilize this property. The same way that we can deduce the dependence of the two series coupled NMOS (NM1, NM4 and NM3, NM5) on temperature in Figure 1. The sources of the two NMOS are connected with each other, so the substrate bias effect can be ignored. In addition that the threshold voltages of two transistors counteract with each other cause the gate-voltage of one subtract that of another.

This way, an output voltage with 0 TC can be achieved through connecting two series coupled NMOS and a single NMOS. Following, we describe the operation of the entire circuit in detail.

According to the figure 1, the output voltage can be express as

$$Vref = V_{GS2} - V_{GS1} + V_{GS4} - V_{GS3} + V_{GS5}$$

$$= V_{TH2} + \xi V_T \ln(\frac{3Iref}{K_2 I_0}) + \xi V_T \ln(\frac{2K_1K_3}{K_4K_5}). \quad (11)$$

$$V_{TH2} = V_{THO} - \kappa T. \quad (12)$$

Where V_{THO} is the threshold voltage at 0 K, and κ is the TC of V_{TH}. The derivation of equation (12) to temperature, the dependence of $Vref$ on temperature is given by

$$\frac{\partial V_{ref}}{\partial T} = -\kappa + \xi\frac{k}{q}\ln(\frac{3Iref}{K_2 I_0}) + \xi\frac{k}{q}\ln(\frac{2K_1K_3}{K_4K_5}). \quad (13)$$

So the TC has a relationship with κ and the aspect ratio of the transistor. While TC equals to 0 K, κ satisfies the expression

$$\kappa = \xi\frac{k}{q}\ln(\frac{3Iref}{K_2 I_0}) + \xi\frac{k}{q}\ln(\frac{2K_1K_3}{K_4K_5}). \quad (14)$$

Associate equations (14) with (11), (12), $Vref$ can be rewritten as

$$Vref = V_{THO}. \quad (15)$$

i.e., reference voltage equals to threshold voltage at 0 K while 0 TC is satisfied.

Based on the analysis above, the temperature compensation of the voltage reference circuit is observed through combining two series coupled NMOS (NM1, NM4 and NM3, NM5) with a single NMOS of deferent TC. In addition, the consideration about current source made us had to think about the influence of the secondary temperature coefficient of the practical resistor. And we can take advantage of this to achieve secondary temperature coefficient correction of reference voltage.

With equations (2), (3) and (13), while m of equation (3) is 1, rewrite equation (2)

$$I_0 = \mu_0 T_0 C_{ox}(\xi - 1)k^2 T / q^2. \quad (16)$$

The dependence of reference voltage on temperature is given by

$$\frac{\partial V_{ref}}{\partial T} = -\kappa + \xi\frac{k}{q}\ln(\frac{3\xi q \ln K_7}{K_2\mu_0 T_0 k C_{0X}(\xi-1)R}) + \xi\frac{k}{q}\ln(\frac{2K_1K_3}{K_4K_5}). \quad (17)$$

The right second item of equation (17) shows that TC of reference voltage is associated with κ, the aspect ratio and the TC of the resistor.

III. SIMULATION RESULTS AND DISCUSSION

Based on SMIC 0.18 μm CMOS process and using Cadence Spectre simulated entire circuit. The layout of the voltage reference circuit and the area is about$(90\times70)\mu m^2$. In condition of 1.8V power supply, the simulation result is shown in figure.2 with a temperature range from -25℃ to

115℃. The temperature variation is 1.32 mV, so the temperature coefficient is 15ppm/℃. We can see the output reference voltage has the secondary temperature coefficient. According to the equation (17) which shows the relationship of the TC of reference voltage with the TC of the resistor, the TC characteristic curve is modulated by the secondary temperature coefficient of the resistor.

Figure.3 shows the output reference voltage V_{ref} at room temperature as a function of supply voltage in a range from 0 to 3V. The voltage reference operated correctly when supply voltage is higher than 0.9V, and the line sensitivity was 0.62mV/V for supply voltages 0.9-3V.

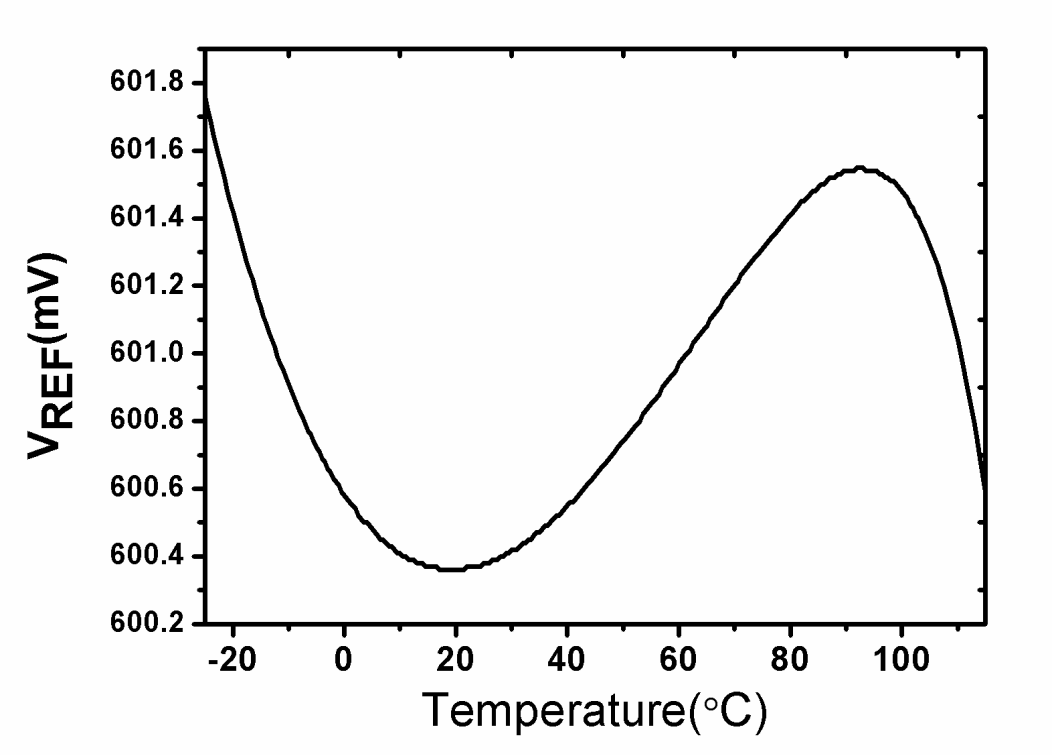

Figure2. The typical temperature coefficient of the voltage reference is 15ppm/℃

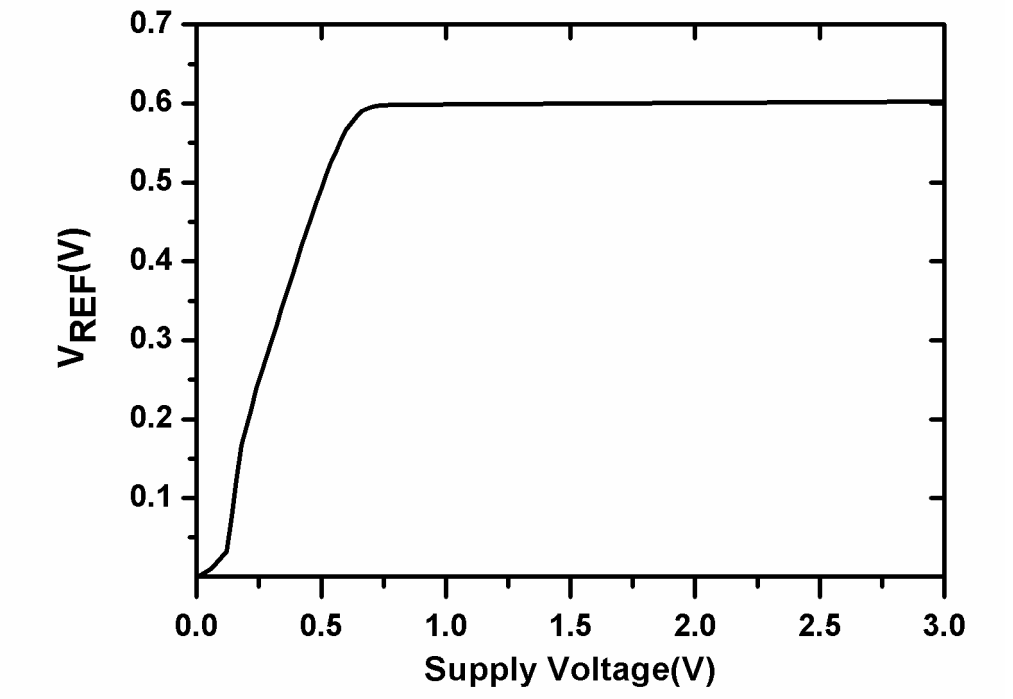

Figure3. The range of supply voltage at room temperature, and line sensitivity was 0.62mV/V for supply voltages 0.9-3V

IV. CONCLUSIONS

Based on SMIC 0.18 μm CMOS process, this article proposed a simple architecture CMOS voltage reference with ultra-low power and low voltage through analyzing the performance of MOS transistor operated in sub-threshold. The TC of the output voltage is 15ppm/℃. The power dissipation is only 0.54 μW under 1.8V power supply. And it has good performance in PSRR of -55dB within 10KHZ.

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