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A Low Noise ASIC for Butterfly Accelerometer

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***Abstract*—An open-loop switch-capacitor detection circuit with high resolution and low noise is proposed for a butterfly accelerometer. This paper introduced the composition and realization principle of the system, proposed a C/V detection structure and a filter with high Q value. The preamplifier adopted the folded cascode structure with the gain enhancement technology to achieve high GBW and improved the phase margin. The input common mode feedback helps to achieve a high linearity detection and have an ideal dynamic detection range. All of the voltage and current are supplied by the reference source with low temperature coefficient. Under the Cadence Design System, the spectre circuit simulation is performed based on the 0.6um CMOS standard process model. The results show the detection range of the Accelerometer is ±0.1pF, sensitivity is 25V/pF, output noise is within 0.4uV/Hz1/2.**

Keywords-butterfly accelerometer; switch-capacitor detection; gain-enhancement; common mode feedback

I. INTRODUCTION

Micro-accelerometer is an important part of the inertial navigation for its measurement of line acceleration. It has dominant position in sensor field for its small size, light weight, low cost, low power dissipation, easy integration, etc [1]. Since the advent of the accelerometer in 1980s, the institution around the world had entered into research. The capacitive micro-accelerometers are widely used owe to its low temperature drift and ideal linearity characteristics[2]. At the same time, switch-capacitance detection method accounted for a large proportion[3][4]. In this paper, an interface circuit for butterfly accelerometer is proposed. By using switch-capacitor detection method and fully differential structure, high gain and low noise detection are realized.

II. MECHANICAL STRUCTURE

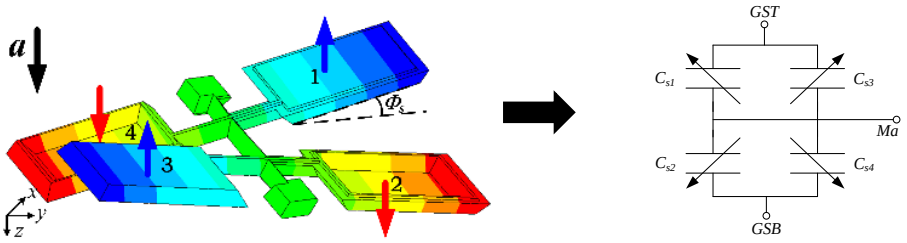


Figure 1. Mechanical structure of the butterfly accelerator

This circuit is designed for the butterfly accelerator based on V-Shape Beam. Its mechanical structure and equivalent capacitance are showed in Fig.1[5], the Ma is public pole, Mass 2,4 have different qualities to mass 1,3.When the accelerometer is affected by an acceleration toward the direction of z, the unbalanced mass will be twisted around the support beam. Since the same mass is cross-symmetrical, the two pairs of non-equilibrium mass twist in the opposite direction. The V-beam structure is used to realize the absolute symmetry of the support frame, which has large bending rigidity and small torsional rigidity. The detection sensitivity of this structure is 16fF/g, its drift in whole temperature range is 5.12mg, the temperature coefficient is 0.051mg/℃, and the temperature sensitivity of the scale factor is 79.9ppm/℃.In order to design an circuit for the accelerometer, some parameters have been concluded as table 1.

TABLE I. PARAMETER OF ACCELEROMETER

Parameter	Value
Sensitivity	16fF/g
Cut-off frequency	1.6kHz
Operation frequency	0~100Hz

III. INTERFACE CIRCUIT

According to the parameters above, the resolution of interface circuit has to be at least order fF, resolution is 25V/pF with 5V voltage supply. Set the cut-off frequency of the low-pass filter slightly larger than 100Hz since the operation frequency is less than 100Hz, and the value about filter can eliminate noise to the greatest extent possible.

Capacitance detection methods are mainly include modulation and demodulation detection and switch-capacitor detection, this paper is based on the switch-capacitor technology, using a fully differential structure, to achieve a high sensitivity, high slew rate, high linearity and low noise interface circuit. The system chart is shown in Fig.2. Variation from capacitance to voltage changes through C/V, switch-capacitor circuit makes signal in high frequency. Sampling with high frequency clock and passing LPF can obtain smooth curve. And using switch-capacitance in C/V, Sampling and Filter can effectively reduce 1/f noise. Reference and Timing are basic modules for entire circuit.

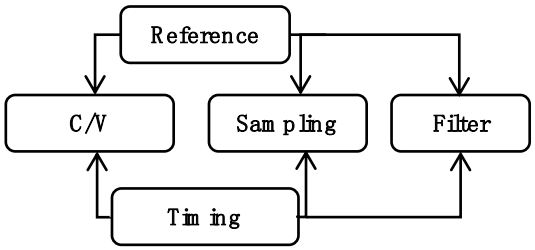


Figure 2. Block diagram of the Circuit

A. *CV Circuit*

Capacitance detection is the first step of surface circuit. Due to the signal capacitance to be measured is weak, pre-stage circuit needs to suppress noise well. The preamplifier plays a critical role for the performance of detection circuit since it is an interface from capacitance to voltage conversion. This part mainly introduces the design of op-amp and optimization of C/V.

a) Preamplifier: High-performance OPAMP is the core circuit in analog integrated circuit. In this paper, the gain-enhancement folded cascode amplifier is used to obtain large input common mode feedback, output voltage swing, impedance so as improve the open-loop gain. The gain and bandwidth of the opamp can be decided by accuracy. The structure and characteristics of operational amplifier is shown in Fig.3, It can be seen that the gain is about 140dB.The second pole of system is away from the GB point and phase margin is about 45 °.

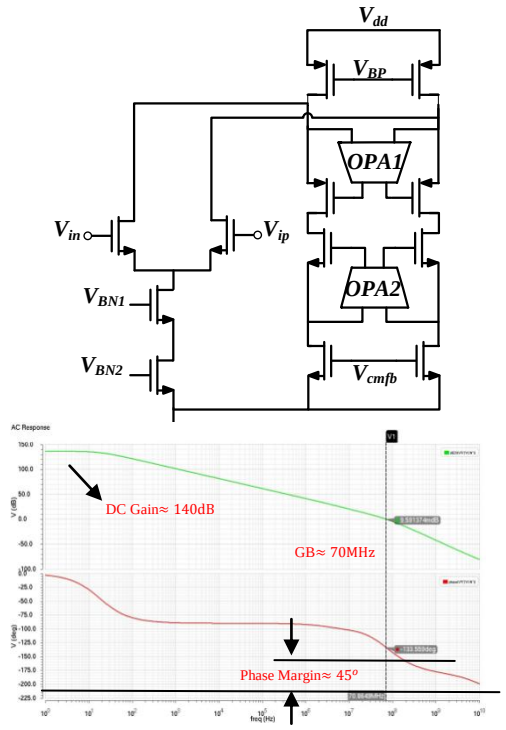
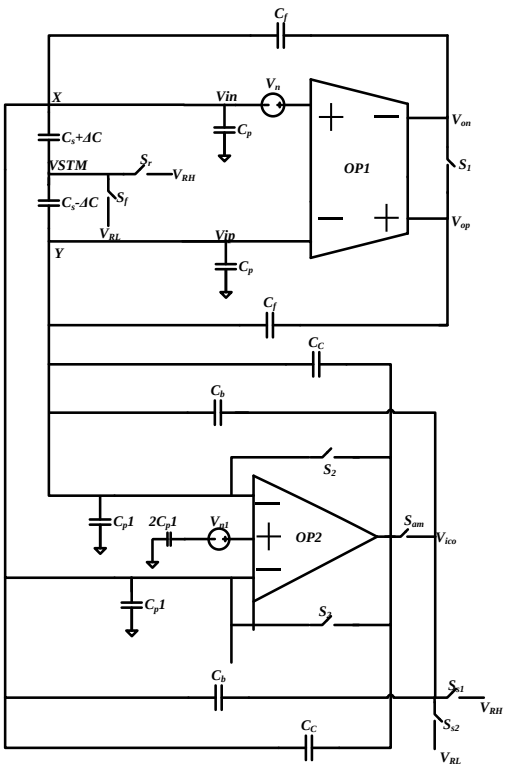


Figure 3. Folded Cascode with gain-boosting and the amplitude-frequency characteristics

b) Structure design: For Common Capacitance detection structure, 3dB bandwidth will be reduced when there is parasitic capacitance between the common plate and capacitance to be measured. We proposed the structure of C/V as shown in Fig.4. This structure has several design points: the use of fully differential structure is to obtain a large voltage swing and suppress the power noise; add the output common mode feedback structure can stabilize the DC operating point, obtain a complete dynamic range; add input CMFB by using auxliary OPAMP to improve linearity. Meanwhile, the main OPAMP with NMOS input level, auxiliary OPAMP with PMOS input stage can make the main OPAMP has a better dynamic range; compensation capacitor can configure the initial state of the capacitor to avoid the structure unmatched. VIN, VIP is the detection signal input. VON,VOP is the main OPAMP output, Cs is the base capacitor, Cf is feedback capacitor of the main OPAMP, control its magnification. Cb is feedback capacitor for the auxiliary operational, is used to configure the common mode point of auxiliary OPAMP output, Cc is the compensation capacitor.

When S1 opened, The public pole of differential capacitance $(C_s + \Delta C)$ and $(C_s + \Delta C)$ is reseted by VRH,the amount charge stored in $(C_s + \Delta C)$ and $(C_s - \Delta C)$ respectively are $(C_s + \Delta C) \times [V_x(\text{reset1}) - \text{VRH}$ and $Cs - \Delta C \times Vxreset1 - VRH$.When S1 closed,the public pole changed to VRL and charge stored in differential capacitance changed to $(C_s + \Delta C) \times [V_x(\text{amp1}) - \text{VRL}]$ and $(C_s - \Delta C) \times [V_x(\text{amp1}) - \text{VRL}]$. In a same way, we can record the charge on other capacitances. List condition of each capacitance as table1:



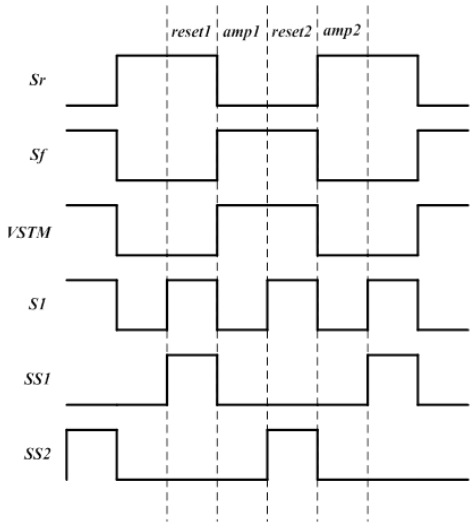


Figure 4. Schematic diagram and timing clock of CV

List condition of each capacitance as Table2:

TABLE II. CAPACITANCE CONDITION FROM RESET1 TO AMP1

Point X	C_f	$C_s + \Delta C$	C_p	C_{p1}	C_b
Reset1	$V_x(S1) - V_{ocm}$	$V_x(S1) - VRL$	$V_x(S1) - 0$	$V_x(S1) - 0$	$V_x(S1) - VRH$
Amp1	$V_x(S0) - V_{op}$	$V_x(S0) - VRH$	$V_x(S0) - 0$	$V_x(S0) - 0$	$V_x(S0) - V_{ico}$

According to the charge conservation, as S1 changing from reset1 to amp1, following relationship can be referred(the input noise and parasitic capacitance are existing):

$$(C_S + \Delta C)(VRL - VRH + V_x(S0) - V_x(S1)) + C_f(V_{ocm} - VOP + V_x(S0) - V_x(S1)) + (C_p + C_{p1})(V_x(S0) - V_x(S1)) + C_b(VRH - V_{ico} + V_x(S0) - V_x(S1)) + (C_c + \Delta C_c)(V_x(S0) - V_{ico}) = 0 \quad (1)$$

Similarly, capacitances about point Y have the same equal relationship:

$$(C_S - \Delta C)\left(VRL - VRH + V_y(S0) - V_y(S1)\right) + C_f\left(V_{ocm} - VON + V_y(S0) - V_y(S1)\right) + \left(C_p + C_{p1}\right)\left(V_y(S0) - V_y(S1)\right) + C_b\left(VRH - V_{ico} + V_y(S0) - V_y(S1)\right) + (C_c - \Delta C_c)(V_y(S0) - V_{ico}) = 0 \quad (2)$$

Combine the basis of the characteristics of OPAMP and charge conservation, differential output is

$$VOP - VON = \frac{2\Delta C}{C_f}(VRL - VRH) + \frac{2\Delta C}{C_f}\left(V_{n1}(S1) - V_{n1}(S0)\right) + \frac{C_s + C_f + C_{p1} + C_b + C_p}{C_f} V_n(S0) \quad (3)$$

It can be inferred from Vout that the output noise of the OPAMP is only related to OP1.At the same time, the capacitance of Cf can be determined by VRH, VRL,Voutmax and capacitance changing according to $C_f = \frac{2\Delta C_{max}}{V_{out\,max}}(VRH - VRL)$.And it can be determined from the Vico that CCM=Cb,C1>>Cp,C2>>Cp1.Besides,the C/V circuit adds an accelerometer offset compensation circuit, controlled by a binary capacitor compensation array.It can compensate capacitor from 20fF to 160fF. The sensitivity of compensation capacitor is:

$$\frac{VOP - VON}{\Delta Cc} = \frac{2(V_{CM} - V_{ico} - V_{n1}(S0))}{Cf} \quad (4)$$

B. Sampling and Filter

Fig.5 shows high frequency outputs from C/V, sample the point in specific frequency so that smooth curve graph can be got. Besides, Sampling causes the signal mixing, the low-frequency noise with useful signal is modulated to high frequency and will be eliminated after LPF.

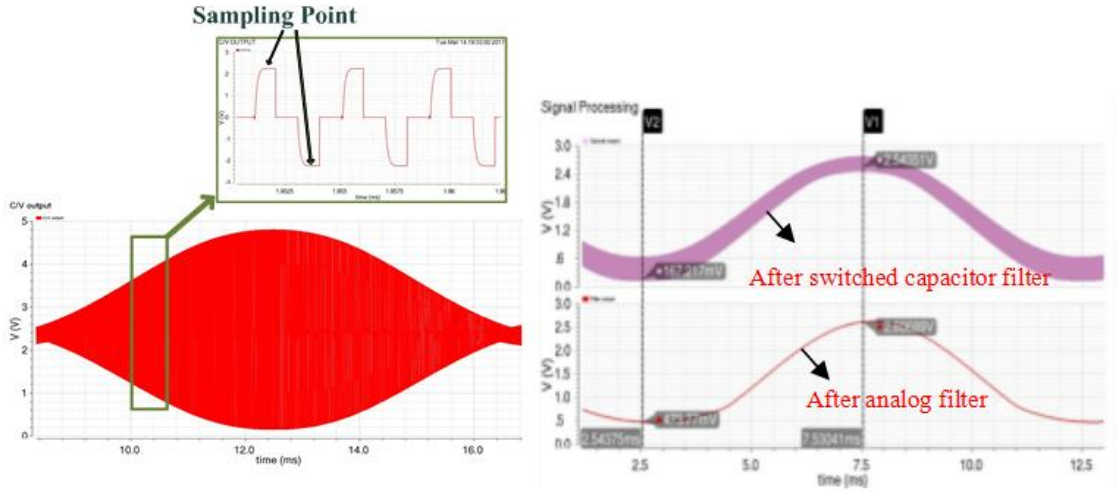


Figure 5. Output after C/V and filter

In order to expand the range of LPF filtering out low-frequency signal, it is necessary to set the cut-off frequency in the useful range as small as possible. A switched capacitor filter is applicable since the using of analog filters brings large capacitor, resistance, unnecessary area and power consumption. An analog filter is used to eliminate the high-frequency noise caused by switching capacitor filter.

Fig.6 is the structure and magnitude-frequency characteristic. The output of the second stage directly go back to the input makes a larger Q value. The CDS circuit can effectively suppress the low frequency component in the fully differential circuit.

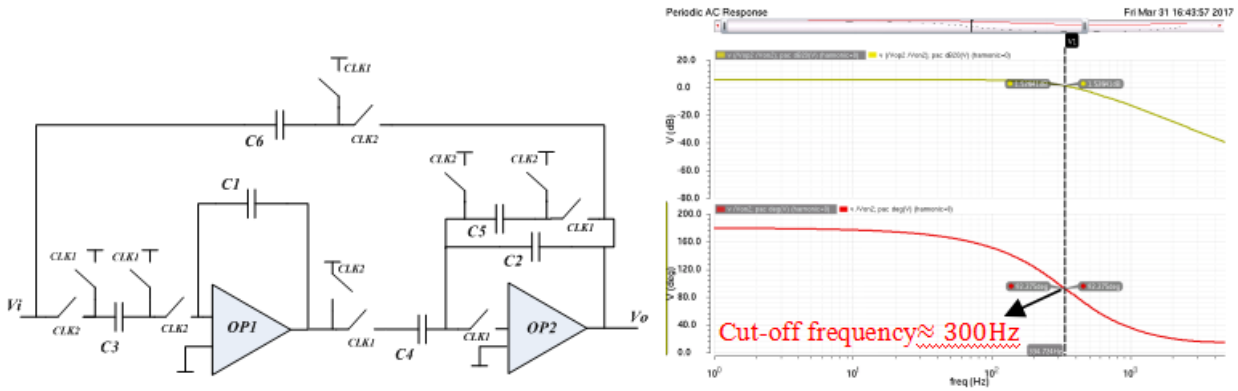


Figure 6. Switch-capacitor filter structure and AC characteristics

IV. Simulation and Testing

As shown in Fig.7, the voltage is measured by different base capacitance values under the same input, it can be seen that the interface circuit with common mode feedback is good in linearity, and the compensation capacitor can be achieved 20f ~ 160f capacitive compensation, the sensitivity is about 14.7V/pf. After filtering out low-frequency signal Fig.8 is the noise comparison of the signal before sampling and output signal. It can be seen the low-frequency noise is effectively eliminated.

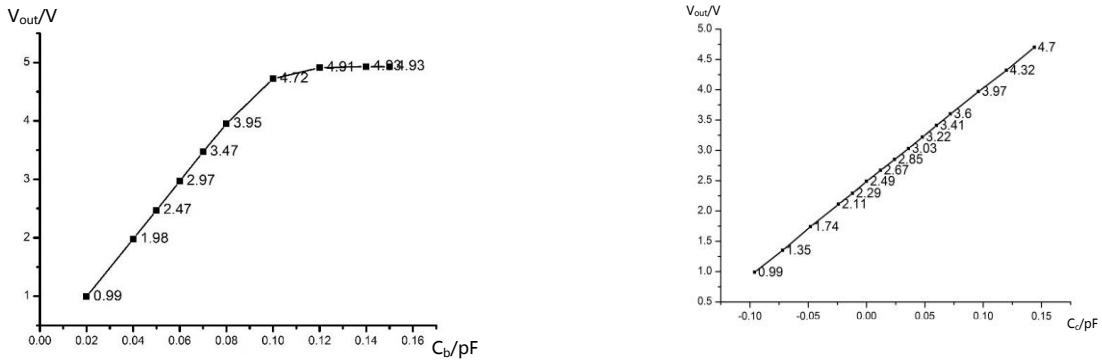


Figure 7. The change of output Voltage due to base capacitor(left) and compensation capacitor(right)

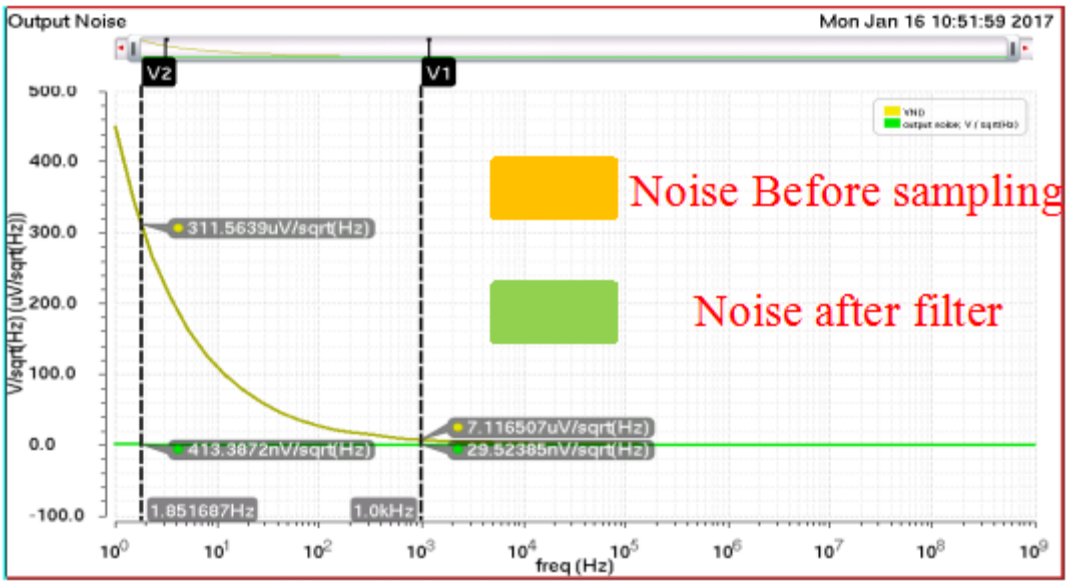


Figure 8. Comparison of noise before sampling and after filter

ACKNOWLEDGMENT

In this paper, a butterfly accelerometer interface circuit is designed with switch-capacitor open-loop detection method. The cascode amplifier with gain-enhanced is used to improve the open-loop gain. Maximize the output swing by selecting the main and auxiliary amplifier correctly of the input mode; Process the signal through two stage filter can eliminate low-frequency noise effectively. Compensation capacitor can configure initial state precisely. Simulation results show that the butterfly accelerometer can measure acceleration form -6g to +6g, the sensitivity is 0.4V/g, output noise is within $0.4uV/Hz^{1/2}$.

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