

Clock Tree Synthesis in ASIC Back-end Design

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Abstract—Based on the Synopsys physical design tool IC Compiler, taking the design of BES6799 chip under SMIC 0.18 μ m Logic 1P5M process as an example, this paper analyzed and compared the clock skew and clock cell area of clock trees which are built by three methods, such as inserting inverter, buffer, combination of both. It was found that the clock tree completed with buffers has a better clock skew and the clock cell areas are almost the same. So buffer is selected as the clock delay cell to build clock tree. In order to further reduce the clock skew and then make timing closure, the clock tree synthesis method which the important clocks are synthesized first is proposed. It was shown that the method can effectively reduce the clock skew and clock cell area. Based on the above methods, the chip was finally taped out in SMIC.

Keyword—clock tree synthesis (cts); clock skew; clock closure; clock cell area

I. INTRODUCTION

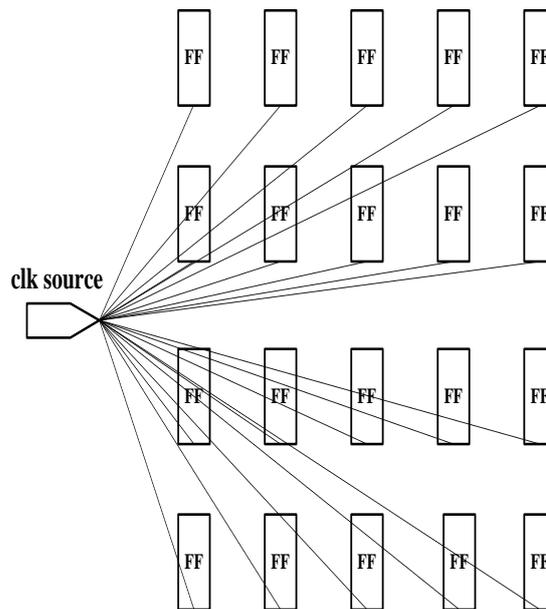
In the design of large-scale digital integrated circuits, the clock signal is the benchmark for data transmission. It plays a decisive role in the function and stability of the synchronous digital system. Therefore, the characteristics of the clock signal and its distribution network are especially concerned.

The clock signal is usually the largest fan-out, the longest passing distance, the highest speed of the signal in the whole chip [1]. Since the distance between all registers controlled by the same clock signal and the clock source is different, the time of clock signal arrived at the CK port of each register is different. The maximum time deviation between different registers is called the clock skew [2]. If the clock skew is too large, it is difficult to optimize timing in the next work. That will lead to insert a lot of delay cells and the circuit power consumption and area will be increased. If the circuit's timing is disturbed, the wrong data signal will be latched into the register that may result in the system function error. Thus, in high-speed ASIC design, clock skew is more and more concerned by the designers. Due to the problem of load capacity, the clock source signal can't directly drive all registers, so clock distribution network mostly uses the clock tree architecture now. How to build a clock tree determines the quality of the circuit clock skew, therefore CTS plays an important role in digital chip back-end design. Taking the BES6799 chip as an example, by comparison and analysis then buffer is selected to build the clock tree and an effective method to reduce the clock skew of clock tree is proposed.

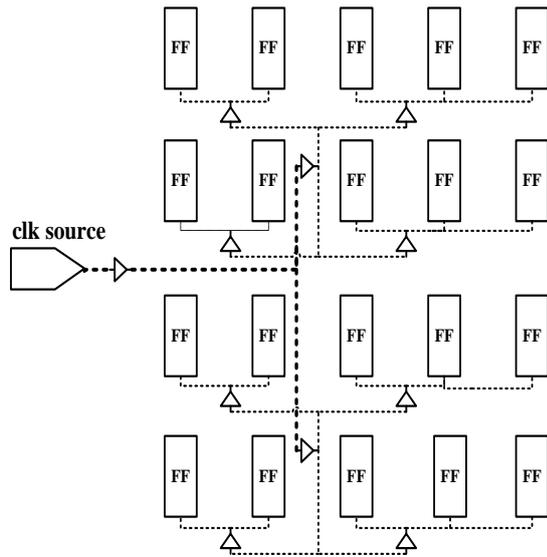
II. THE CLOCK TREE SYNTHESIS CONCEPT

Starting from the clock source, the clock buffer or inverter is inserted to separate the fan-out and adjust the delay of the clock signal. This construction of clock distribution network is called CTS. The CTS is aimed at improving the problem of high fan-out and clock skew. The two most important goals are the minimization of clock skew and phase delay, and the optimization of power consumption of clock network [3].

As shown in Figure 1 is clock network before or after CTS, where Figure 1(a) is clock network before CTS and Figure 1(b) is clock network after CTS. As can be seen from Figure 1, after CTS the high fan-out has been obviously alleviated, while the buffer series has been increased.



(a). Clock network before CTS



(b). Clock network after CTS

Figure 1. Clock network before or after CTS [4]

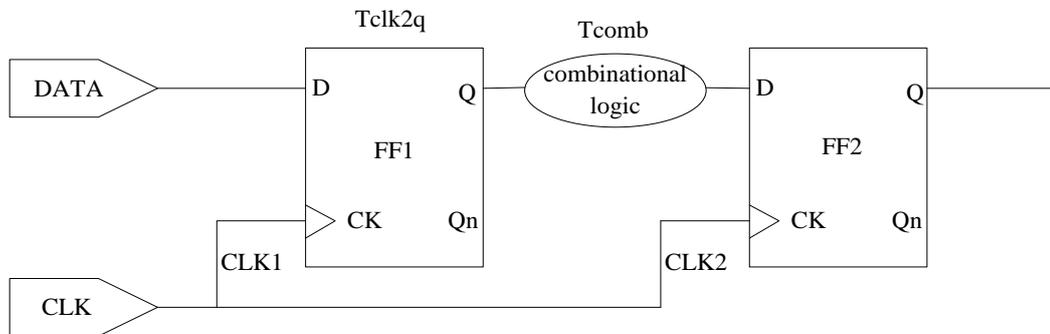


Figure 2. Setup/hold time analysis model

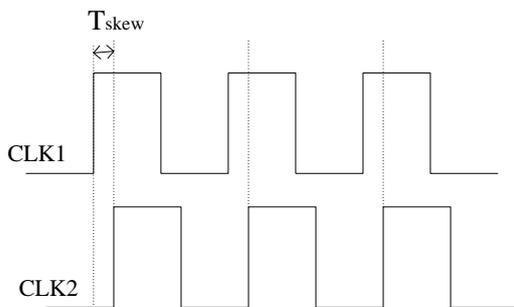


Figure 3. Clock skew waveform

For the T_{setup} , it must meet,
 $T + T_{skew} \geq T_{clk2q} + T_{comb} + T_{setup}$.

(1) If formula (1) is not met, it is called a setup time violation.

For the T_{hold} , it must meet,
 $T_{hold} + T_{skew} \leq T_{clk2q} + T_{comb}$.

(2) If formula (2) is not met, it is called a hold time violation.

As can be seen from formula (1), when T , T_{clk2q} and T_{comb} are fixed, if T_{skew} is positive, that is, the clock path delay of FF2 is longer than FF1, the T_{setup} is easy to meet. In this case, formula (2) is not easy to meet that may

The condition for normal operation of the sequential circuit is to satisfy the constraint between setup time (T_{setup}), hold time (T_{hold}) and clock cycle of registers. As shown in Figure 2 is setup/hold time analysis model, where T_{setup} is that the register data input data needs to be held for a while before the valid clock edge is arrival. And T_{hold} is that the register data input data needs to be held for a while after the valid clock edge is arrival. In the figure, T_{clk2q} is the delay of the register, and T_{comb} is the delay of the combinational logic circuit.

As the practical circuit has clock skew, as shown in Figure 3, T_{setup} and T_{hold} of register are not easy to meet the timing requirement.

cause a hold time violation and result in function error. On the contrary, if T_{skew} is negative, the T_{hold} is easy to meet, while the T_{setup} is not easy to meet, that may also cause function error. And the T_{setup} , T_{hold} , T_{clk2q} are related to the structure and property of the device itself, depending on the improvement of the process to further reduce, so reducing T_{skew} becomes an important part of the back-end design and the key to improve the speed of the circuit. So the traditional CTS method will take "zero clock skew" as the goal of clock synthesis [5].

CTS is a very important step in completing timing closure. Based on the Synopsys physical design tool IC Compiler, taking the design of BES6799 chip under SMIC 0.18 μ m Logic 1P5M process as an example, by comparison and analysis then buffer is selected to build the clock tree and an effective method to reduce the clock skew of clock tree is proposed.

III. THE CLOCK TREE SYNTHESIS INSTANCE

The BES6799 chip was integrated by digital modules and analog modules, and the design scale is about 75,000. The operating frequency is mainly 8MHz and 12MHz. It was taped out successfully in SMIC. The clock structure is shown in Figure 4.

An external crystal oscillator provides a reference clock source (CLK_12M) for the chip. One way is multiplied through the internal PLL circuit to get the clock

(CLK_60M), and then through a divide-by-two frequency divider to get the clock (CLK_30M). The other way is connected to a multiplexer. The internal oscillator generates a clock source (CLK_32M). One way passes a divide-by-four frequency divider to get a clock (CLK_8M). The other way is connected to a multiplexer. While the SCK and SCK_n are the clock used for the SPI communication system, the frequency is about 8MHz. A special register is clocked by the rising edge of SAR_SS_PAD. The frequency of SS is extremely low, which is about 500 kHz.

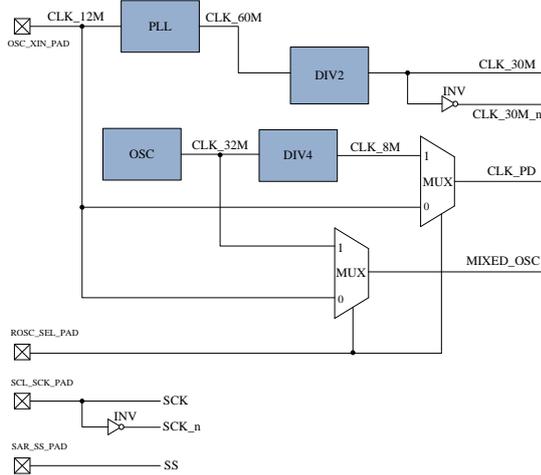


Figure 4. Clock structure in BES6799 chip

The chip has two operating modes, Normal mode and Scan mode. In the Normal mode, the system clock is determined by CLK_PD. In the Scan mode, the system uses the three clocks, SCK, SS and MIXED_OSC. As the timing of the Scan mode is relatively easy to meet, so the main concern is whether the timing of the Normal mode meets the requirement during CTS. The reports given below are also reported in Normal mode.

In CTS, the order and constraints will affect the final result. There are three main methods of CTS, inserting inverter or buffer or combination of both. In order to find a better way, we build the clock tree by inserting inverter, buffer and the combination of both, respectively. And then the clock skew and clock cell area of clock trees which are built by the three methods are compared, the comparison results are shown in Table 1 and Table 2. Table 1 shows that the clock skew of inserting buffer is better. Table 2 shows that the clock cell area of inserting inverter is smaller, but the clock cell areas of the three methods are not much difference, relative to the whole chip area. Since the aim of CTS is to reduce clock skew and then make the timing closure. Thus, the buffer is selected to build clock tree as clock delay cell, after consideration.

TABLE I. CLOCK SKEW REPORTS OF THREE METHODS

Clock	Inverter(ns)	Buffer(ns)	Combination of both(ns)
CLK_12M	0.2752	0.2281	0.2654
CLK_32M	0.2484	0.2100	0.2274
CLK_60M	0.2537	0.2245	0.3015
SCK_CLK	0.3383	0.3058	0.3341
SS_CLK	0.0050	0.0090	0.0052
CLK_8M	0.2695	0.2527	0.2898
CLK_30M	0.2638	0.2367	0.2791
CLK_PD	0.2929	0.2189	0.2273

TABLE II. CLOCK CELL AREA REPORTS OF THREE METHODS

Clock	Inverter(μm^2)	Buffer(μm^2)	Combination of both(μm^2)
CLK_12M	1623.8206	1783.7574	1800.6913
CLK_32M	3381.2334	2846.8604	2630.4758
CLK_60M	1125.1967	1896.6532	1450.7137
SCK_CLK	16.9344	16.9344	16.9344
SS_CLK	62.0928	62.0928	62.0928
CLK_8M	1454.4763	1631.3474	1638.2817
CLK_30M	681.1392	1172.2368	730.0607
CLK_PD	1454.4763	1631.3474	1648.2817
Total clock cell area	9799.3697	11041.2298	9977.5221

For the sake of better timing closure, taking into consideration that the BES6799 chip has two important clocks CLK_12M and CLK_32M, we proposed a method

to synthesize important clocks first beside inserting buffer.

Important clocks synthesis first command is as follows, `compile_clock_tree -clock_trees {CLK_12M CLK_32M}`.

TABLE III. CLOCK SKEW AND CLOCK CELL AREA REPORTS OF IMPORTANT CLOCKS SYNTHESIS FIRST METHOD

Clock	clock skew(ns)	clock cell area(μm^2)
CLK_12M	0.2080	1486.4640
CLK_32M	0.1849	1853.3767
CLK_60M	0.2250	1962.5094
SCK_CLK	0.2939	16.9344
SS_CLK	0.0042	62.0928
CLK_8M	0.2340	1334.0543
CLK_30M	0.2255	1002.8926
CLK_PD	0.2141	1334.0543
Total clock cell area		9052.3785

Table 3 shows the clock skew and clock cell area reports after building clock tree with the important clocks synthesis first method. By comparing the clock skew and clock cell area of inserting buffer in Table 1 and Table 2, it can be found that the result of the important clocks synthesis first method is obviously superior to directly inserting buffer. The clock skews of CLK_12M, CLK_32M, SCK_CLK, SS_CLK, CLK_8M, CLK_30M, CLK_PD were reduced by 8.81%, 11.95%, 3.89%, 53.33%, 7.40%, 4.73%, 2.19%. And the clock cell area was reduced by 18.01%. Therefore, using important clocks synthesis first method to build clock tree can effectively reduce the clock skew and clock cell area.

IV. CONCLUSION

With the device size reduced to deep sub-micron stage, clock skew has become a key factor affecting the performance of ASIC chips. Taking the CTS of the BES6799 chip as an example, this paper analyzed the mechanism and influence of the clock skew and the appropriate delay cell was selected to reduce the clock skew by comparison. Finally, based on the buffer as delay cell and using important clocks synthesis first method to build clock tree, the clock skew and clock cell area are obviously reduced. It lays a good foundation for the next work.

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