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Mutual Compensation of Threshold Voltage and Thermal Voltage Temperature Effects with Applications in Voltage Reference Generator

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***Abstract*—A low power, low temperature coefficient (TC) CMOS voltage reference generator is proposed in this paper, which exploits temperature mutual compensation relationship between threshold voltage and thermal voltage, and provides a mean reference voltage of 411.8mV.In this reference, a proportional to absolute temperature (PTAT) current containing the thermal voltage which has a positive TC is generated, and then it is injected into a diode-connected NMOS transistor that supply the threshold voltage which has a negative TC. The mixing of the two voltages produces a reference voltage with zero TC. The proposed circuit is verified by SPICE simulation with CMOS 0.18um process technology. The simulation results show that the power consumption is 17.9nW and the TC is 8.6ppm/℃. The proposed circuit is suitable for power sensitive applications.**

Keywords-voltage reference; low power; low tc; cmos; thermal voltage

I. INTRODUCTION

RFID tag are used numerous in medical field, they are attached to the medical apparatus and instruments to register, track and monitor them [1]. Tags used in the medical field need to be able to work under high temperature, because these devices like surgical instruments should be sterilized by high temperature and high pressure with a temperature about 121~134 degrees. Meanwhile, Passive systems require lower power consumption. For this purpose, many kinds of voltage reference circuits are proposed. For example, some advanced bandgap voltage reference based on parasitic bipolar transistor have lower power consumption than the traditional bandgap reference are invented [2, 3], but they are not performs satisfactorily because of the parasitic bipolar transistor in a standard CMOS process is usually not very well characterized. Meanwhile, many nanopower voltage reference circuits based on the fact that the threshold voltage of MOSFETs with different gate oxide thickness in the same CMOS technology exhibit different temperature characteristic are proposed [4, 5, 6, 7], but such solutions also can not be implemented in a standard CMOS technology because they require additional fabrication steps. Besides, a novel voltage reference was introduced in [8, 9, 10], these devices consist of standard MOSFETs operating in subthreshold regime. It generates a MOSFET threshold voltage with negative TC and a multiple of the thermal voltage with positive TC, and then adds them to produce a voltage reference with zero TC, but they either have high TC [8], or have high power consumption [9], or both have [10]. Besides it can not applicable at high temperature [9, 10].

To solve the above mentioned problems, a novel voltage reference circuit is presented in this paper. It generates a PTAT current containing the thermal voltage with a positive TC and then injected into a diode-connected NMOS transistor which supplies the threshold voltage with a negative TC to achieve an output voltage reference near zero TC. Simulation results show that this work has low power dissipation, low TC and high temperature.

II. PROPOSED CIRCUIT

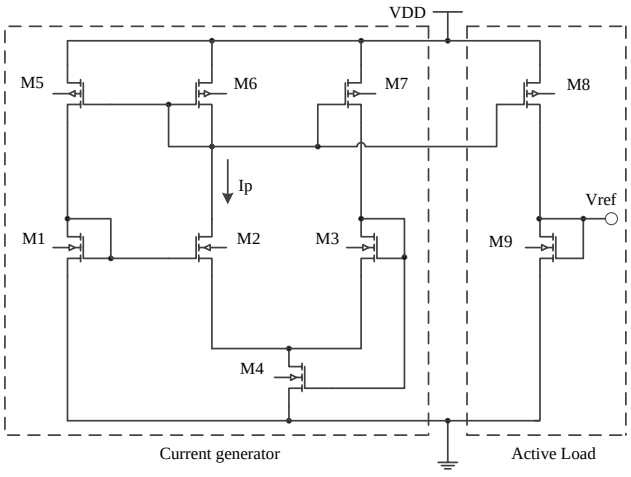

Figure 1. Proposed voltage reference circuit

The architecture of the proposed voltage reference is shown in Fig. 1. It consists of a current generator and an active load. Start-up circuit is ignored here. The current generator generates a PTAT current I_P , and then injected

into the active load that include a diode-connected transistor to generate the reference voltage V_{ref}. All the MOSFETs except for M3, M4 and M9 are operated in the subthreshold region. The MOSFET M4 is operated in the strong-inversion and deep triode region, and the MOSFET M3 and M9 are operated in the saturation.

A. Current Generator Circuit

The current-voltage characteristics of a MOSFET that operates in the subthreshold region can be approximated by Eq. (1).

$$I_D = KI_0 \exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right)\times\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right] \quad (1)$$

where K is the aspect ratio ($=\frac{W}{L}$) of the transistor (W and L are the channel width and length), V_{GS} and V_{DS} are the gate-source voltage and the drain- source voltage, respectively. $I_0 = \mu C_{ox}\frac{W}{L}(m-1)V_T^2$, μ is the electron mobility in the channel, C_{ox} is the gate-oxide capacitance, V_T ($=\frac{K_B T}{q}$) is the thermal voltage (K_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge), V_{TH} is the threshold voltage, and m is the subthreshold slope factor.

The current generator can generate the current I_P without using a resistance. This is extremely important if the current I_P need to be very small, to drastically reduce the power consumption of the circuit. In such case a large resistance would be required causing a large area occupation on the chip. The channel length modulation effect of M4 is negligible since it is long channel devices. Besides, the drain-source voltage in M4 is very small by setting the parameter, thus the MOSFETs M1 and M2 have larger drain-source voltage than their thermal voltage. As $V_{DS} \geq 0.1V$, current I_D is almost independent of V_{DS} and given by Eq. (2)[9].

$$I_D = KI_0 \exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right) \quad (2)$$

The current I_P can be derived through the following steps. From Fig. 1 the drain-source voltage V_{DS4} is given by Eq. (3).

$$V_{DS4} = V_{GS1} - V_{GS2} \quad (3)$$

From Eq. (2), we arrive at the expression:

$$V_{GS} = V_{TH} + mV_T \ln\left(\frac{I_D}{KI_0}\right) \quad (4)$$

Because the transistor M5 and M6 consist of current mirror, the current in M1 is $\frac{K_5}{K_6}I_P$. Therefore, the voltage V_{DS4} can be expressed as:

$$V_{DS4} = mV_T \ln\left(\frac{K_5 K_2}{K_6 K_1}\right) \quad (5)$$

The channel length between transistors pairs (M5-M8, M1-M2, and M3-M4) are designed equally to reduce the threshold voltage mismatch.

Due to M3 operated in saturation and M4 operated in a strong-inversion, deep-triode region, the drain current in M3 and M4 can be expressed as:

$$I_3 = \frac{1}{2}\mu_n C_{ox} K_3 \left(V_{GS3}-V_{TH}\right)^2 \quad (6)$$

$$I_4 = \mu_n C_{ox} K_4 \left(V_{GS3}-V_{TH}+\frac{1}{2}V_{DS4}\right)V_{DS4} \quad (7)$$

The MOSFET M7 copy the current I_P in proportion from M6, consequently the current in M3 is $\frac{K_7}{K_6}I_P$, and the current in M4 is the sum of the current in M2 and M4. Rewrite the above two expressions we have:

$$\frac{K_7}{K_6}I_P = \frac{1}{2}\mu_n C_{ox} K_3 \left(V_{GS3}-V_{TH}\right)^2 \quad (8)$$

$$\left(1+\frac{K_7}{K_6}\right)I_P = \mu_n C_{ox} K_4 \left(V_{GS3}-V_{TH}+\frac{1}{2}V_{DS4}\right)V_{DS4} \quad (9)$$

Combine the Eq. (8) and Eq. (9), we can obtain that:

$$V_{GS3}-V_{TH} = K + \sqrt{K+K^2}V_{DS4} \quad (10)$$

where $K = \frac{K_4 K_7}{K_3 (K_6 + K_7)}$. Then substituting Eq. (5) and Eq. (10) in Eq. (8), the PTAT current I_P is obtained as:

$$I_P = \frac{1}{2}\mu_n C_{ox} \frac{K_3 K_6}{K_7}\left(K + \sqrt{K + K^2}\right)^2 m^2 V_T^2 \ln^2\left(\frac{K_5 K_2}{K_6 K_1}\right) \quad (11)$$

From the Eq. (11), it can be seen that a current contains the thermal voltage is obtained, we can inject it into a diode-connected transistor to compensate the threshold voltage, then a zero TC reference voltage can be generated.

B. Active Load

Because the diode-connected transistor M9 working in the saturation region, the reference voltage can be expressed as:

$$V_{ref} = V_{th4} + \sqrt{\frac{2I_9}{\mu_n C_{ox} K_4}} \quad (12)$$

The generated current I_P is mirrored into a diode-connected transistor M9. The current in M9 can be expressed as $I_9 = \frac{K_8}{K_6} I_P$, thus the Eq. (12) becomes:

$$V_{ref} = V_{th4} + \sqrt{\frac{2K_8}{K_6 K_4}\frac{I_P}{\mu_n C_{ox} K_4}} \quad (13)$$

Substituting Eq. (11) in Eq. (13), and the reference voltage V_{ref} is given by:

$$V_{ref} = V_{th4} + \sqrt{\frac{K_8 K_3}{K_7 K_4}}\left(K + \sqrt{K + K^2}\right) m V_T \ln\left(\frac{K_5 K_2}{K_6 K_1}\right) \quad (14)$$

where $K = \frac{K_4 K_7}{K_3 (K_6 + K_7)}$.

C. Temperature Compensation

From the Eq. (13), we can see that V_{ref} consists by V_{th4} which has a negative TC and V_T which has a positive TC. So a zero TC reference voltage can be obtained by adjusting the coefficients in front of V_T.

The temperature dependence of the threshold voltage can be given by:

$$V_{TH}(T) = V_{TH}(T_0) + \alpha(T - T_0) \quad (15)$$

where T_0 is the reference temperature which is $300°K$ and α is a negative value [11], substituting Eq. (15) and $V_T = \frac{K_B T}{q}$ in Eq. (14), the reference voltage V_{ref} can be rewritten as:

$$V_{ref} = V_{th4}(T_0) + \alpha(T - T_0) + m\frac{K_B T}{q}\sqrt{\frac{K_8 K_3}{K_7 K_4}}\left(K + \sqrt{K + K^2}\right)\ln\left(\frac{K_5 K_2}{K_6 K_1}\right) \quad (16)$$

By differentiating Eq. (16) with respect to the temperature, we obtain:

$$\frac{\partial V_{ref}}{\partial T} = \alpha + m\frac{K_B}{q}\sqrt{\frac{K_8 K_3}{K_7 K_4}}\left(K + \sqrt{K + K^2}\right)\ln\left(\frac{K_5 K_2}{K_6 K_1}\right) \quad (17)$$

By setting Eq. (17) to zero, we obtain the condition:

$$-\alpha = m\frac{K_B}{q}\sqrt{\frac{K_8 K_3}{K_7 K_4}}\left(K + \sqrt{K + K^2}\right)\ln\left(\frac{K_5 K_2}{K_6 K_1}\right) \quad (18)$$

Therefore, if Eq. (18) is satisfied, a zero TC reference voltage can be obtained. From Eq. (16) and Eq. (18), the reference voltage V_{ref} is expressed as:

$$V_{ref} = V_{TH4}(T_0) \quad (19)$$

therefore, the circuit generates the threshold voltage of MOSFET at absolute zero temperature.

D. Simulation Results

To verify the performance of the proposed design, we use the SPICE simulator to simulate the circuit with SMIC 0.18um CMOS process. Fig. 2 shows a plot of the measured output voltages versus temperature with a range from 0℃ to150℃, the calculated TC is 8.6ppm/℃ at VDD=0.7V. Fig. 3 shows the voltage reference V_{ref} as a function of power supply from 0V to 1.8V at room temperature, with a supply line sensitivity (LS) of about 1.96%/V. Fig. 4 shows the simulation result of PSRR of the voltage reference V_{ref} when T=20℃ and VDD=0.7V. The PSRR without any filtering capacitor is -80dB at 100Hz and -51.7dB at 10MHz, therefore the proposed circuit has a better PSRR performance. Fig. 5 shows the proposed circuit generates a mean reference voltage of about 415.7mV with a variation of 3.9mV at four different power supply voltage: 0.7V, 1V, 1.4V, and 1.8V. Fig. 6 shows the reference V_{ref} at all corners. Fig. 7 shows the TC from 0℃ to150℃ at all corners, the TC of the TT corner is 8.6ppm/℃, and those of the FF, FS, SF and SS corners are 22.2 ppm/℃, 8.9 ppm/℃, 14.7 ppm/℃ and 35.7 ppm/℃, respectively. Fig. 8 shows

the measured power consumption across temperature, the results shows the power increases by 4mW for every 10 degrees increase in temperature. Fig. 9 shows the measured power consumption across supply voltage. The total power consumption of the proposed circuit is 17.9nW at 0.7V power supply and at room temperature. To verify the stability of the circuit operation with process variations. Monte Carlo analysis assuming WID mismatch variations in all MOSFETs were considered. Fig. 10 shows the distribution of average output voltage V_{ref} at 0.7V power supply and room temperature. We assumed a Gaussian distribution (δ_{vth}) for the WID variation. The average voltage V_{ref} was about 411.7012mV in this simulation. The coefficient of variation (δ/μ) in 270 runs was 0.27%. Table I summarize the main performance of the proposed circuit and compares with previous works. As this table reveals, the proposed circuit operates with low TC, low power consumption and high PSRR.

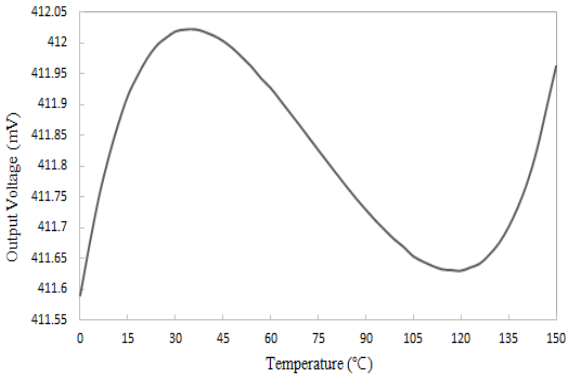

Figure 2. The output reference voltage V_{ref} versus temperature

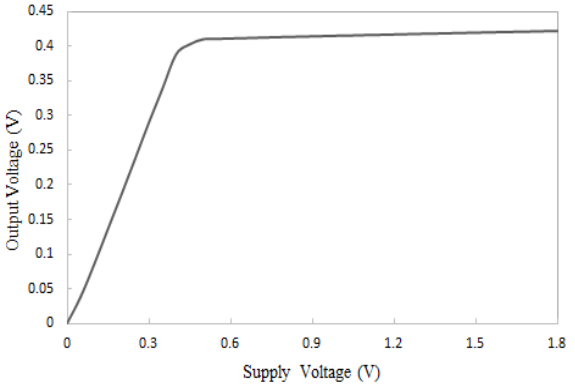

Figure 3. The output reference voltage V_{ref} versus supply voltage

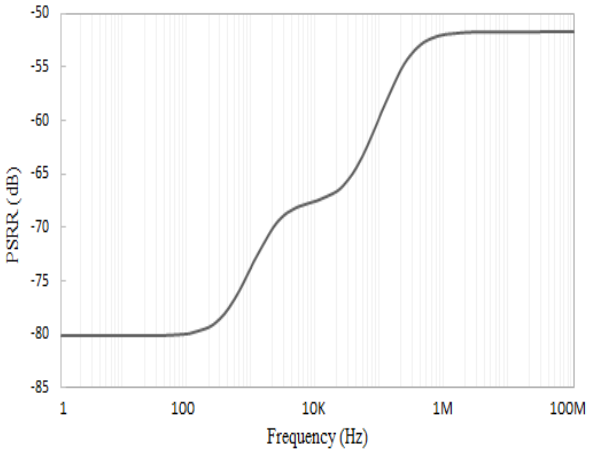

Figure 4. The PSRR at room temperature and a 0.7V supply power

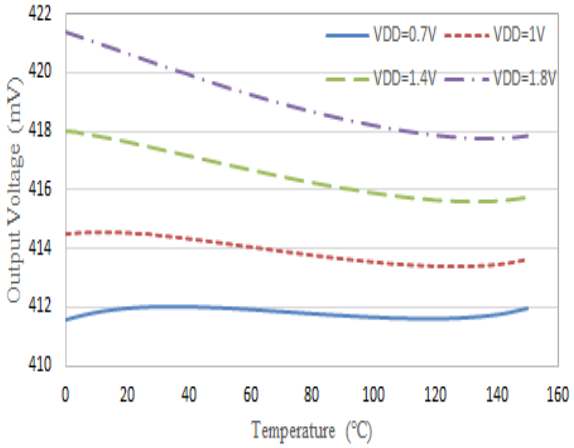

Figure 5. The output voltage reference V_{ref} as a function of temperature at different

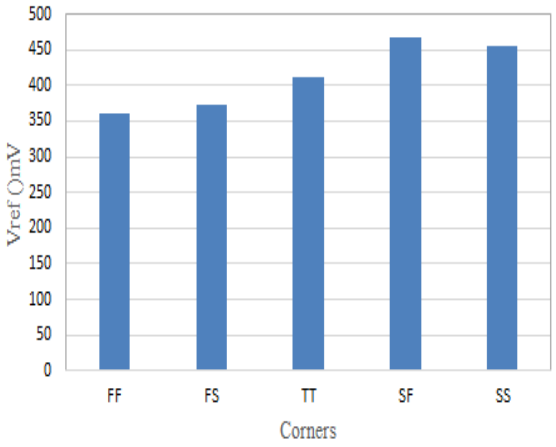

Figure 6. Measured V_{ref} at all corners

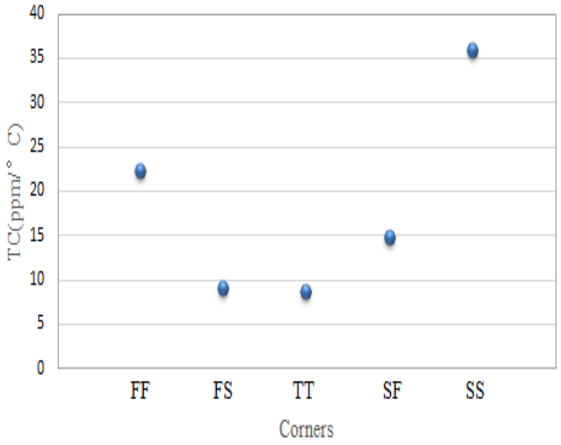

Figure 7. Measured TC at all corners

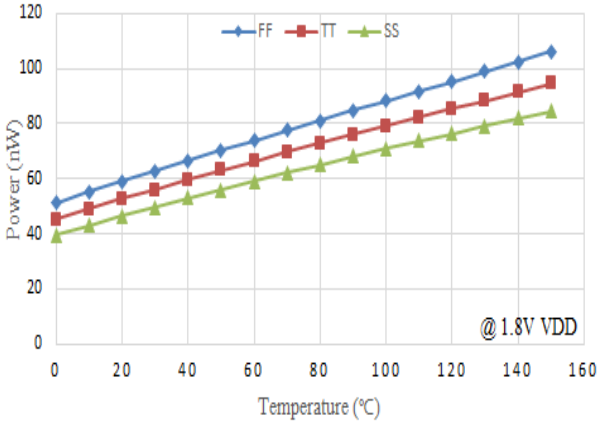

Figure 8. Measured power across temperature

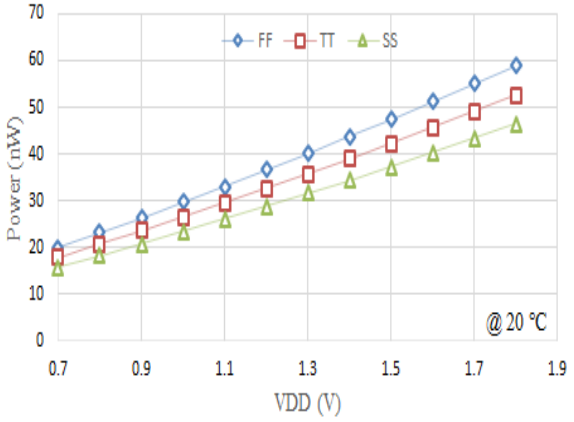

Figure 9. Measured power across VDD

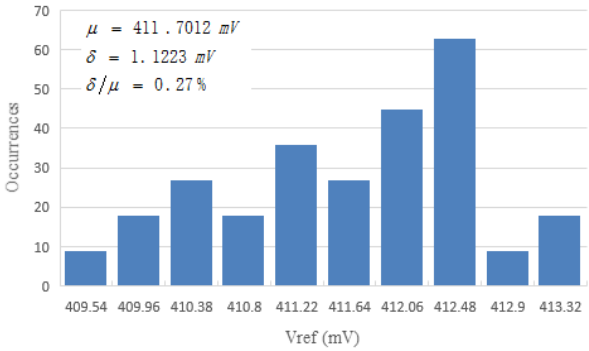

Figure 10. Fig. 10. Distribution of output voltage for 270-point Monte Carlo simulations assuming WID variations

TABLE I. PERFORMANCE COMPARISON

	This work	[7]	[8]	[9]	[10]
Process	0.18 um	0.18 um	0.18 um	0.35 um	0.18 um
Temp range (℃)	0~150	0~125	-10~150	-20~80	-40~120
VDD(V)	0.7~1.8	0.45~2	0.6~2.2	1.4~4	1~3
Vref(mV)	411.8	263.5	650	745	610
Power(nW)	17.9@Room temp	2.6@Room temp	5.1@ Room temp	300@Room temp	230@Room temp
TC(ppm/℃)	8.6	142	37	7	66.9
PSRR	-80dB@100Hz -51.7dB@10MHz	-65dB@100Hz -50dB@1KHz	-40dB@1KHz -62dB@10MHz	-45dB @100Hz	-15.45dB @10MHz

III. CONCLUSION

Our study presents a novel approach for low power, low TC and high temperature voltage reference. The design conditions to minimize the power consumption and the TC have been described in detail. The voltage reference has been implemented in SMIC 0.18-um CMOS process. The results of simulation show that a TC of 8.6ppm/℃ from 0℃ to 150℃, and power consumption of 17.9nW are achieved with a supply voltage of 0.7V. It indicates that the circuit can realize low power and low TC at the same time. Obviously the proposed circuit is suitable for power sensitive large scale integrated circuits such as portable mobile devices, life-assist medical devices and smart sensor. Meanwhile this circuit also suitable for high temperature working environment, like RFID tags in the medical field.

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