The Design of High Impedance S/H Switch in Power-off State

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Abstract: Some times, the input-port of a single supply A/D converter needs a high impedance S/H switch when it does not supply power. Now we introduce a digital logical circuit to realize it. Through this digital logical circuit, when analog input signal is more than 0V, the analog input port to power or ground will be on high impedance state. At the same time, the analog input port also will be on high impedance state to another analog input port in power-off state.

1. Introduction

For getting better safety performance, some key devices in the engineering project always need a backup device to prevent the whole system from working because of some key device breakdown.

For A/D converter, a typical application is as Fig. 1.

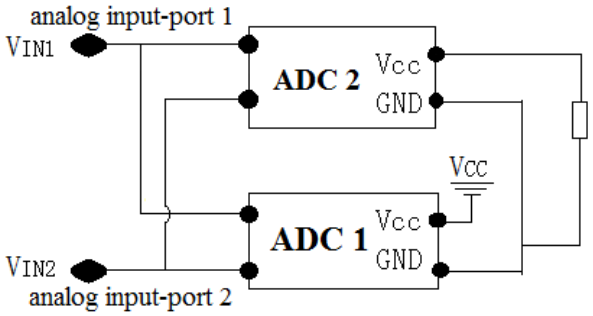

Fig. 1 The typical application diagram

In Fig.1, ADC1 and ADC2 are the same A/D converter, they use the same analog input signal. But in normal condition, ADC1 is on power-up state and ADC2 is on power-off state.

So we should design a single supply A/D converter. It should be on high impedance between different analog input-ports, and the analog input-port to power or ground also should be on high impedance state, when it haves the normal analog input voltage but does not supply power

2. The circuit of digital-logical circuit S/H switch

2.1 The function block diagram of S/H switch

In Fig.2, VDD is the power of A/D converter. GS is the ground of A/D converter. But the digital-logical circuit in switch, all digital-logical units' power is VS and ground is the same with GS. The VS is produced by a series diode through VDD.

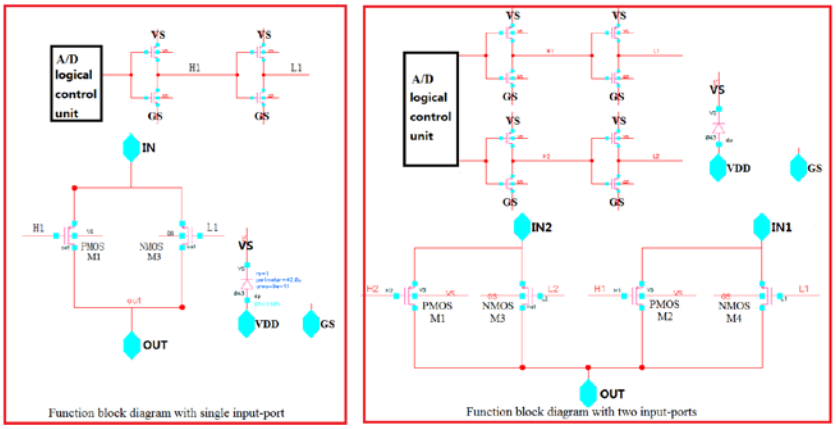

Fig. 2 Function block diagram of S/H switch

2.2 Introduction of application conditions

We design this A/D converter on a standard COMS process. Because of user's request for application, we should design a multi-pass way ADC. Because the user does not use only one ADC at the same time, we must ensure the one ADC which does not work should not effects the other ones. So we should design an ADC which should be on high impedance between analog input port with ground, power and other analog input ports.

It is easy to design the high impedance switch in power-up model, so we only should design one switch which is on high impedance in power-off model.

Because it is a single +5V supply A/D converter, and the analog input signal is 0~5V. We only should be guarantee that it is on high impedance switch when $V_{in} \geqslant 0V$.

Next we should analysis the reason how it ensures the high impedance state, when it's input voltage is greater than 0V in power-off model.

3. The analysis of theory

3.1 Theory analysis for the resistance between input-port with VDD and GS of S/H switch in power-off model

3.1.1 The theory sectional drawing of PMOS and NMOS

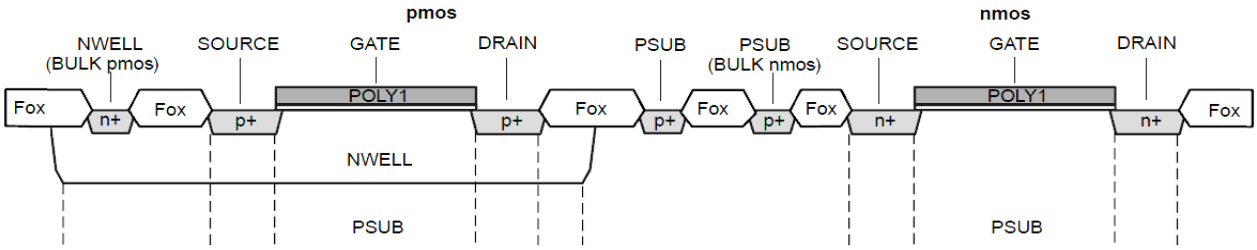

Fig. 3 The theory sectional drawing of PMOS and NMOS

In Fig.3, we can know that the Source to Bulk of the PMOS is approximately equal to a forward biased diode. The Source to Bulk of the PMOS is approximately equal to a back biased diode.

3.1.2 The resistance between input-port with A/D's power and ground

In Fig. 2, when the A/D converter is the power-off state, VDD is approximately equal to 0V. At the same time, the connected relation between input-port with VDD and GS is as shown in Fig.4

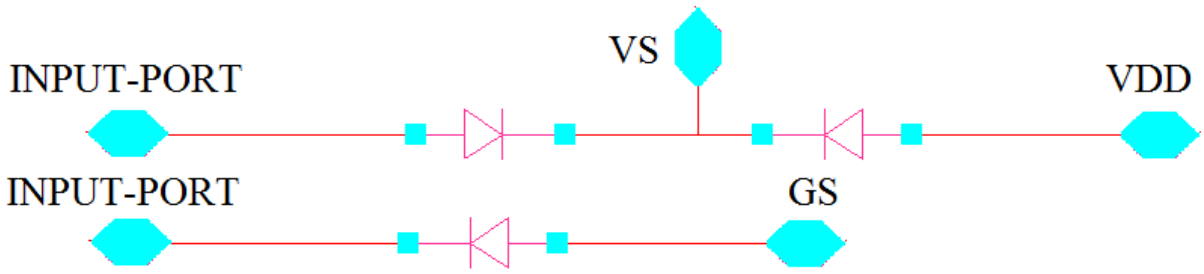

Fig. 4 The equal model between inputport with VDD and GS in power-off model

3.1.3 Conclusion

In Fig. 4, we know that it is on high impedance between input port with VDD and GS when input voltage is greater than 0V.

3.2 Theory analysis for the resistance in different input-ports of S/H switch in power-off model

When the A/D converter is the power-off state, VDD and GS are all approximately equal to 0V. Now all A/D logical control units' output voltage is 0V. The S/H switch' equivalent state is as Fig. 5.

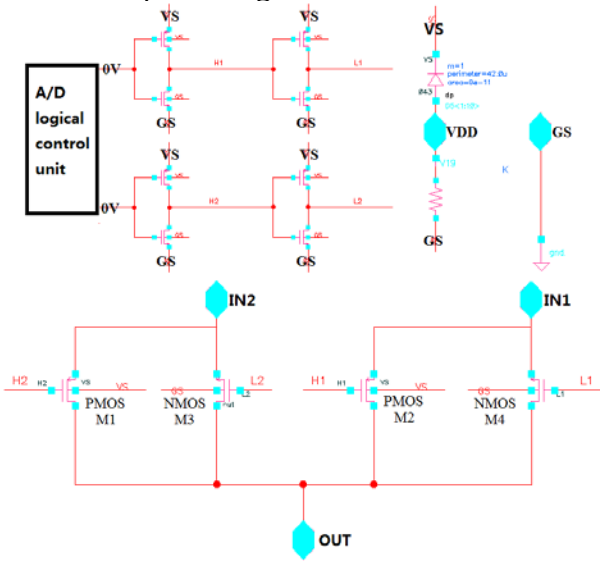

Fig. 5 The equivalent state in power-off model

3.2.1 The relationship between V_{in} with V_H and V_L

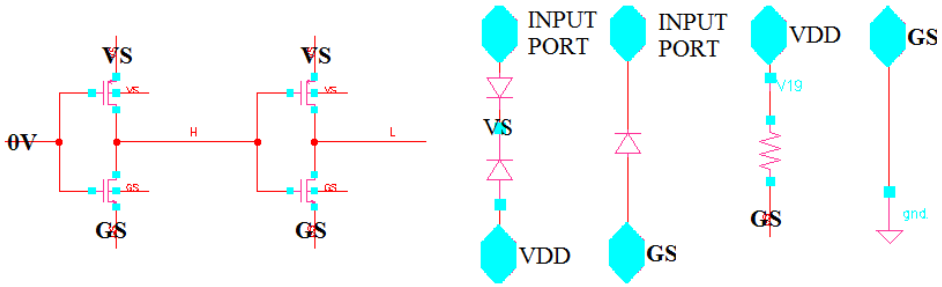

Fig. 6 The equivalent state in power-off model

In Fig.6, V_{on} is the voltage of forward turn-on voltage of diode, V_{th} is the voltage of turn-on voltage of MOS device

when $0V \leqslant V_{in} \leqslant V_{on}$, $V_{vs}=0V$. When $V_{in} > V_{on}$, $V_{vs}= V_{in}-V_{on}$. So $V_{vs} > 0V$ when V_{in} is greater than 0V.

When $0V \leqslant V_{in} \leqslant V_{th}$, $V_{vs}=0V$, $V_H=V_L=0V$. when $V_{vs} \geqslant V_{th}$, $V_H=V_{vs}$, $V_L=V_{GS}$.

Now we can get the conclusion:

When $0V \leqslant V_{in} \leqslant V_{on} + V_{th}$, $V_H=V_L=0V$. (1)

When $V_{in} > V_{on} + V_{th}$, $V_H= V_{vs}$, $V_L=V_{GS}=0V$. (2)

Next we should discuss that there weather is any pass way in different input ports.

3.2.2 The NMOS circuit equivalent state in different input-ports in power-off state

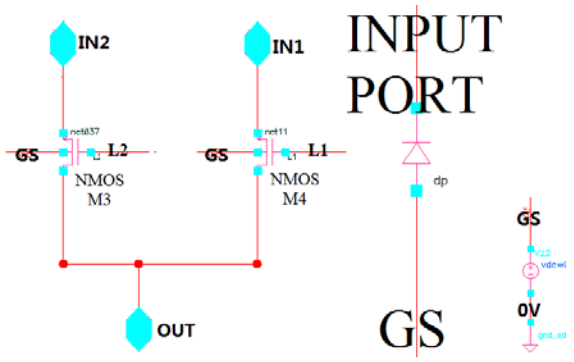

Fig. 7 The NMOS circuit equivalent state in different input-ports in power-off state.

In Fig. 7 and part 3.2.1's conclusion, we can get the conclusion: When V_{in} is positive voltage, $V_{L1}=V_{L2}=V_{GS}$. So when input voltage is greater than 0V. All of NMOS are shut-down model. There is not any pass way in NMOS circuit between different input-ports in power-off model.

3.2.3 The PMOS circuit equivalent state in different input-ports in power-off state

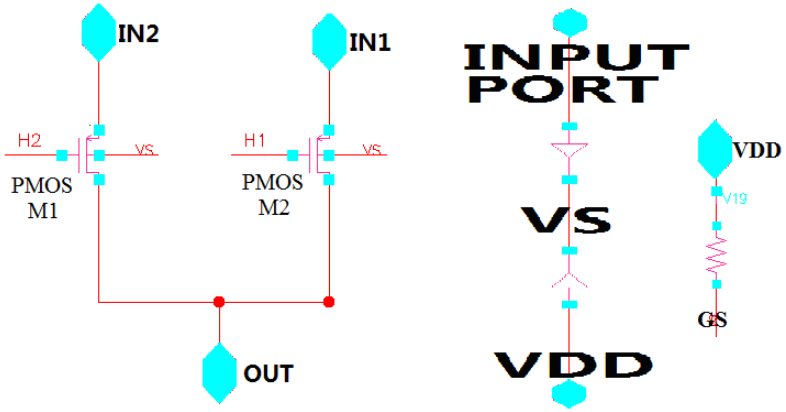

Fig. 8 The PMOS circuit equivalent state in different input-ports in power-off state.

In Fig. 8 and part 3.2.1's conclusion, we can get the conclusion: When $0V \leqslant V_{in} \leqslant V_{on} + V_{th}$, $V_{vs}-V_H \leqslant V_{th}$. When $V_{in} > V_{on} + V_{th}$, $V_{vs}-V_H=0V \leqslant V_{th}$. So when input voltage is greater than 0V, all of PMOS are shut-down model, and there is not any pass way in PMOS circuit between different input-ports in power-off model.

3.2.4 Conclusion

Through the above analysis: There is not any pass way in different input ports. In other word, it is on high impedance between different input ports in power-off model, when input voltage is greater than 0V.

4. The simulation and verification

Through the above theory analysis, this digital-logical circuit S/H switch can realizes the high impedance state in power-off model in theory, so next we should verify it in simulation.

It is not easy to directly test the resistance in simulation, so we only give a linear voltage in analog input port, and test the current in ground, power and other analog input ports. If the current is enough

smaller, we can say that there is not any pass way between analog input-port with the test point. In other word, it is on high impedance state between analog input-port with the test point in power-off state.

The simulation schematic in power-off state is the same with Fig. 9

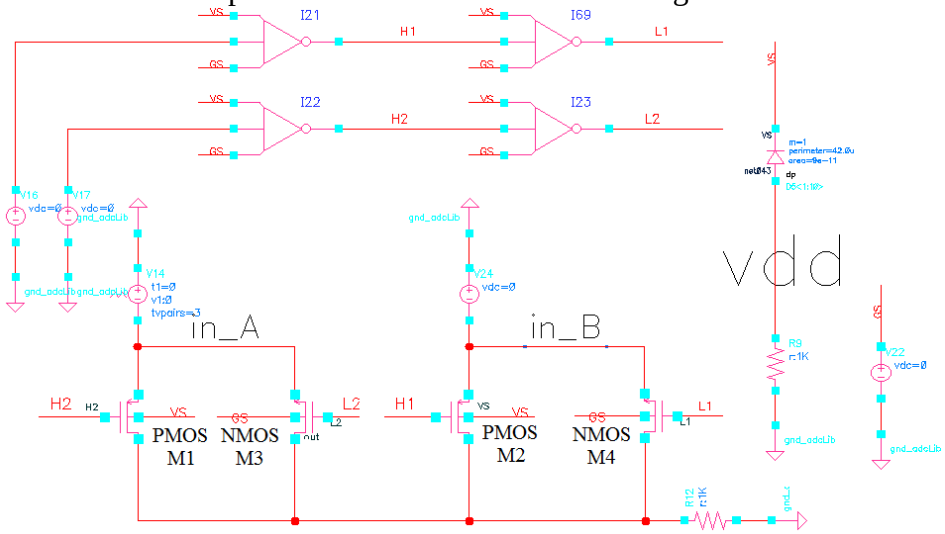

Fig. 9 the simulation schematic between analog input-port with the ground, the power and other analog input port

4.1 The simulation current between analog input-port with the ground

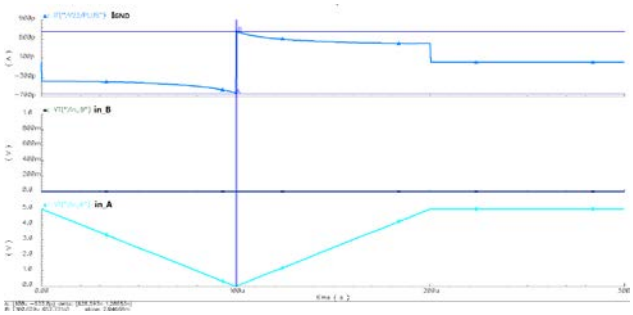

Fig. 10 the simulation current between analog input-ports with the ground

In Fig. 10, the current in the ground is always smaller than 1nA, and the analog input voltage is always smaller than 5V, so we can get the conclusion that the resistance between analog input-port with the ground is smaller than $5V/1nA=5*10^9=5G\Omega$. In other word, it is on high impedance state between analog input-port with the ground in power-off state.

4.2 The simulation current between analog input-port with the power

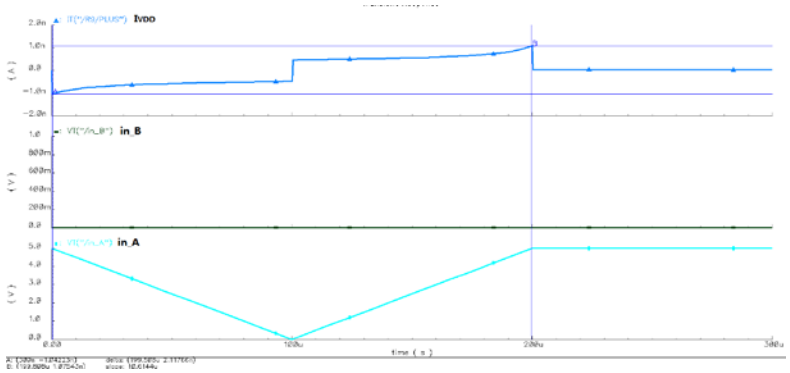

Fig. 11 the simulation current between analog input-ports with the power

As the same with the analysis between input-port with the ground, we can get the conclusion that the resistance between analog input-port with the power is smaller than 5V/1nA=5*10^9=5GΩ. So it is on high impedance state between analog input-port with the power in power-off state.

4.3 The simulation current in different analog input-ports

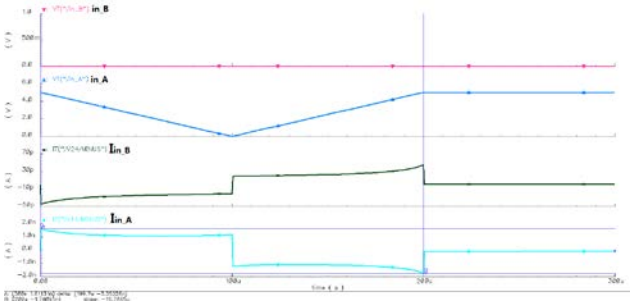

Fig. 12 the simulation current in different analog input-ports

As the same with the analysis between input-port with the ground, we can get the conclusion that the resistance in different analog input-ports is smaller than 5V/2nA=2.5*10^9=2.5GΩ. So it is on high impedance state between different analog input-ports in power-off state.

5. The finished circuit test

Through a standard CMOS process, we get the finished A/D converter circuit by this structure. Now we should test the resistance between input-port with ground, power and another input-port. Because those three resistances are independent, we use the way as Fig.13 to test the minimum value of those three resistances.

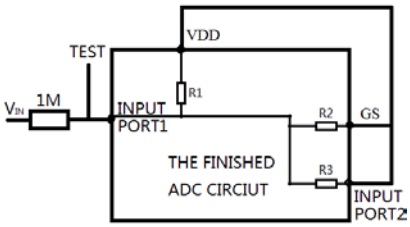

Fig. 13 the circuit diagram of resistance test

In Fig. 13, R1~R3 are the equal resistance between INPUT-PORT1 with VDD, GS and INPUT-PORT2. So we short the above ports as a common port, the resistance(R) between INPUT-PORT1 and the common port is smaller than anyone of R1~R3. Now we only test the R, if the R is enough larger, we can say that it is on high impedance state between INPUT-PORT1 with VDD, GS and INPUT-PORT2 in power-off state.

As Fig.13, we can get: $R=V_{TEST} / (V_{in}-V_{TEST})$. The actual test data is as shown in Table I.

Table 1 The actual test data

V_{in}(V)	V_{TEST}(V)	R(MΩ)
5.0	4.995	999
4.5	4.496	1124
4.0	3.997	1332
3.5	3.498	1749
3.0	2.998	1499
2.5	2.499	2499
2.0	1.999	1999
1.5	1.499	1499
1.0	0.999	999
0.5	0.499	499

As Table 1, we can get the conclusion that the finished circuit is on high impedance state between INPUT-PORT1 with VDD, GS and INPUT-PORT2 in power-off state.

6. Conclusions

By using this structure of A/D converter, the master and slave machines can independently work. So we can realize that when slave machine is on power-off state, the analog input signal in master machine will not be attenuation.

7. Acknowledgments

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