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A Resistorless Voltage Reference with High-order Temperature Curvature Compensation in 55 nm CMOS Process

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Abstract: This paper presents a temperature/supply stable and resistorless voltage reference for high-precision portable electronic products. the reference obtains a good temperature coefficient over a wide temperature range through high-order curvature compensation. In order to reduce the temperature nonlinearity, the piecewise linear temperature curvature compensation circuit is used. The voltage reference is simulated with 55nm CMOS technology. It operates at the voltage of 2.5V and generates a stable voltage at 0.742V with a minimal temperature coefficient of 3.19ppm/℃ for temperature ranging from - 40 to 125℃.

1. Introduction

Precision voltage reference circuits are necessary for the accurate operation of mixed and analog integrated circuits, such as oscillators, PLLs, Data Converters and Dynamic Random Access Memories (DRAM's). These voltage references should be insensitive to variations in process, temperature and supply voltage [1-6]. The performance of many mixed analog/digital systems is limited by inaccuracies and power supply noise coupling errors in integrated voltage references. So precision voltage reference circuits are an integral part of almost all integrated circuit designs.

Many researches have been carried out on high-performance reference circuits with low temperature coefficient (TC) and high PSRR operation [7-10]. Conventional voltage references are based on bandgap reference (BGR) circuit, which is one of the most fundamental building blocks in integrated circuits [11-12]. A BGR voltage is usually composed of a weighted sum of V_{BE} and thermal voltage. However, due to the nonlinear temperature behavior of V_{BE}, curvature compensation approaches are essential for realization of high-precision reference voltage. Some references make use of MOSFETs instead of bipolar junction transistor (BJT) combined with poly-resistor to achieve temperature compensation [13-15]. However, only the first-order resistor TC was considered. Although the second-order TC of resistor is two orders of magnitude smaller than the first-order TC, impact of the former is no less or even larger than the latter when the circuits operate in an environment with temperature higher than 100℃.

In this paper, high-order temperature curvature compensation circuits (HOTCCC) are used to reduce the temperature drift of the reference and to achieve a good TC over a wide temperature range. The proposed technique employs subtraction circuits to compensate curvatures in different temperature ranges. The post simulation results indicate that the proposed curvature-compensation reference improves the TC from 28.5 to 3.19ppm/℃ over a temperature range of −40 to 125℃. The precision of output voltage achieves a line regulation performance of 0.06mV/V for input between 2.25 and 2.75V. The circuit operates at supply voltages down to 2.5V and occupies 270μm × 70μm in standard HLMC 55nm 1P6M CMOS technology.

The remainder of this paper is organized as follows. In section 2 we will describe the principal operation of voltage reference. Section 3 describes the proposed high-precision reference, which

contains a voltage reference with first-order temperature compensation and the proposed TC compensation circuit. Section 4 presents the simulation results, which confirm the effectiveness of the proposed TC compensation. Conclusions are provided in Section 5.

2. Principle of Proposed Voltage Reference

Most related studies used the threshold voltage and carrier mobility of MOSFETs to implement temperature-independent reference circuits. The reference voltage can be expressed as

$$V_{REF} = V_{TH} + AV_{PTAT} \tag{1}$$

where V_{TH} is the threshold voltage of MOSFETs; AV_{PTAT} is a weighted PTAT voltage; which is proportional to μT^2; and μ is carrier mobility of MOSFETs. In the ideal condition, a zero-TC voltage V_{REF} can be achieved. Due to the nonlinear temperature characteristics, high-precision output voltage cannot be achieved without high-order temperature compensation.

Taking into consideration of the effect of nonlinearity temperature components, a resistorless voltage reference with TC compensation is proposed in this paper, as shown in Figure 1. The reference voltage is the sum of the PTAT voltage and CTAT voltage. The PTAT voltage is proportional to ΔV_{GS}, which is proportional to T. By this method, a PTAT voltage with positive linear temperature dependence is successfully obtained. On the other hand, ΔV_{GS} is a function of TC compensation current I_{NTC}. Through adjusting I_{NTC} in different temperature ranges, the temperature slope of the reference voltage can be varied in this range. The CTAT voltage in this paper is formed with the voltage V_g, which is the sum of threshold voltage V_{TH} and the drain-source voltage V_{DS}. Compared with [16], the addition of V_{DS} alleviates design difficulty of PTAT voltage. Details are as described in section 3. The PTAT/CTAT voltage generation and TC compensation are all biased by the biasing current, I_{BIAS}.

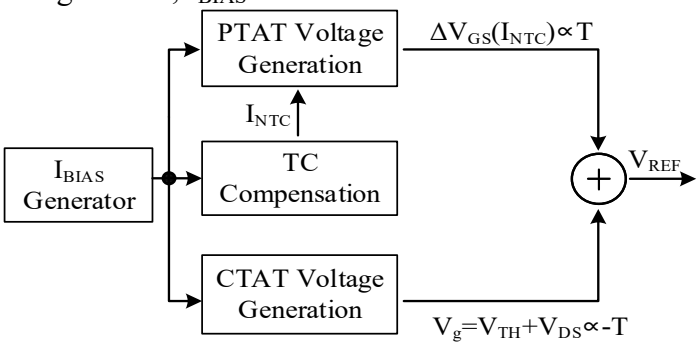

Figure 1. Systematic block diagrams of the proposed voltage reference.

3. Circuit of proposed voltage reference

3.1. Reference circuit with first-order temperature compensation

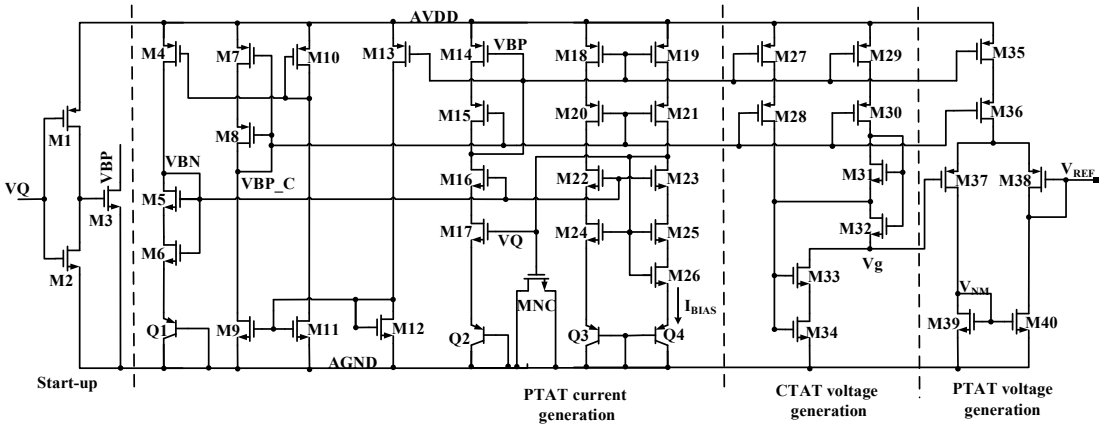

Figure 2. The circuit schematic with first-order temperature compensation.

The reference circuit with first-order temperature compensation is shown in Figure 2. All of the MOSFETs are biased in the strong inversion region without requirement of subthreshold operations. As shown in Figure 2, the PTAT current I_{BIAS} can be expressed as

$$I_{BIAS} = V_{TH} \ln(N) \mu C_{ox} S_{M26} (V_{GS,M26} - V_{TH,M26}) \tag{3}$$

where C_{OX} is the gate-oxide capacitance per unit area; N is the emitter area ratio of transistors Q4 and Q3; V_T is the thermal voltage kT/q; k is Boltzmann's constant; and q is electron charge; S_i is the aspect ratio of transistor i; $V_{GS,M26}$ is the gate-source voltage of M26.

In Figure 2, the CTAT voltage is form by MOSFETs M27-M34. All of the transistors, except M32 and M34, work in the saturation region. Transistor M32 and M34 are biased in the triode region. Given $S_{M27}=2S_{M29}$, and $S_{M33}=3S_{M31}=3S_{M32}$, the overdrive voltage of M31 and M33 should be equal. The output voltage, V_g, can be expressed as

$$V_g = V_{TH,M33} + V_{DS,M34} \tag{4}$$

where $V_{TH,M33}$ is the threshold voltage of M33 and $V_{DS,M34}$ is the drain-source voltage of M34, which can be expressed as

$$V_{DS,M34} = 3V_T \ln(N) \times \frac{S_{M26}}{S_{M34}} \times \frac{V_{GS,M26} - V_{TH}}{V_{GS,M34} - V_{TH}} \tag{5}$$

From (5), it should be noted that $V_{DS,M34}$ shows linearly positive temperature behavior. By adjusting the size of M34 appropriately, the temperature slope of CTAT voltage is reduced which benefits to the design of PTAT voltage.

The PTAT voltage generated circuits as shown in Figure 2, according to the characteristics of MOSFETs in the saturation region, the voltage difference between the gates of M37 and M38 can be described as

$$\Delta V_{GS} = \sqrt{2/\mu C_{ox}} \left(\sqrt{I_{M37}/S_{M37}} - \sqrt{I_{M38}/S_{M38}} \right) \tag{6}$$

From [15], ΔV_{SG} could be rewritten as

$$\Delta V_{GS} = \delta T \tag{7}$$

where δ is a temperature-independent constant, which could be rewritten as

$$\delta = \sqrt{A \frac{S_{M26}}{S_{M37}}} - \sqrt{B \frac{S_{M26}}{S_{M38}}} \tag{8}$$

where A and B are constants. As shown in (4), the voltage $V_{DS,M34}$ reduces the temperature slope of PTAT voltage. From (2), the temperature slope of ΔV_{GS} also reduces to generate zero TC reference voltage. Since the temperature slope of ΔV_{GS} decreases, the difference between sizes of M37 and M38 also decrease, which improves the stability of the circuit. The greater the difference between sizes of M37 and M38 is, the higher the risk of M38 going into the subthreshold region.

Combining (4) and (6), the output voltage of the proposed voltage reference, V_{REF}, can be given by

$$V_{REF} = V_g + \Delta V_{GS} = V_{TH,M33} + V_{DS,M34} + \Delta V_{GS} \tag{9}$$

Therefore, a resistorless temperature-stable reference voltage can be achieved in the proposed configuration. However, due to the process variations, the reference voltage with first-order compensation may not meet the requirement.

Transistor M4-M13 and Q1 provide the Biasing voltage (VBP, VBP_C), as shown in Figure 2. The start-up circuit is made up of transistors M1-M3. When the proposed voltage reference is powered on, the voltage at node VQ is lowed to turn M1 on. The gate voltage of M3 increases. When the gate voltage of M3 is high enough to turn on M3, the voltage at node VBP is pulled down, and there are currents flowing into the circuit of PTAT part to set up proper operating points. At the same time, the voltage at node VQ increases slowly. When VQ increases high enough to turn on M2, M1 will be turned off, and M3 will enter the deep linear region. Thus, the proposed PTAT circuit can successfully avoid degenerating states without extra power consumption and influencing the normal operation of the current generator in steady state.

3.2. Proposed TC Compensation Circuit for Reference Voltage

As mentioned above, the proposed reference comprises a reference part and a TC compensation part. The TC compensation part modifies the slope variation of the TC currents at different temperature ranges. Furthermore, operation currents of MOS transistors change slightly with temperature.

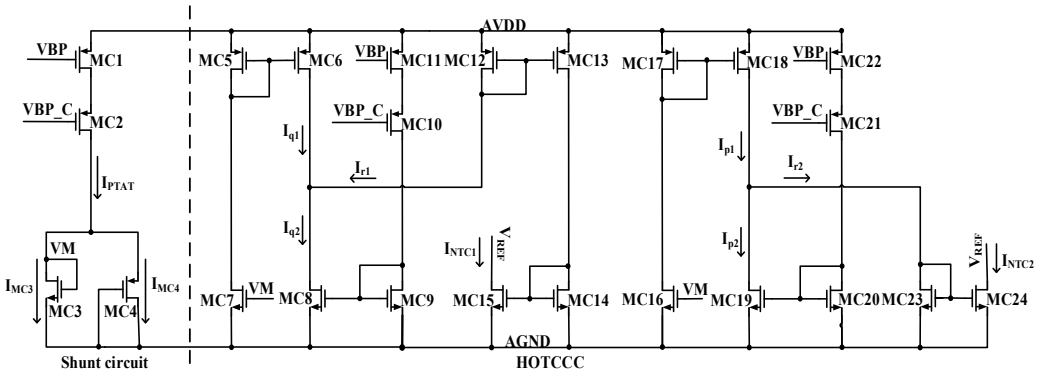

Figure 3. The proposed TC Compensation Circuit.

As shown in Figure 3, the proposed TC compensation circuit has two sub-parts: shunt circuit, and HOTCCC. The shunt circuit is shown in the left part of Figure 3, MC3 and MC4 are both diodes connection. The currents in MC3 and MC4 are negatively dependent on TC. Therefore, through adjusting the size of the MC3 and MC4, a CTAT current can be obtained, as shown in Figure 4.

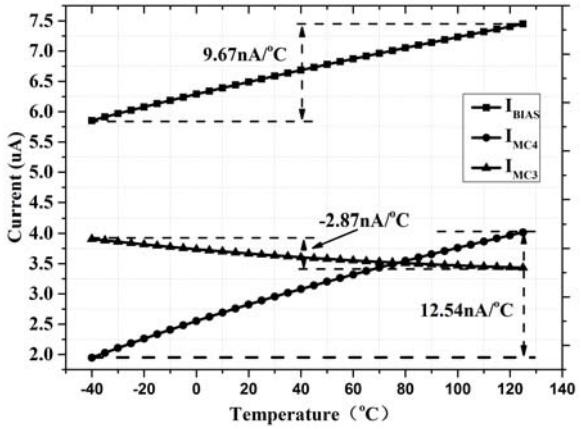

Figure 4. The output current versus temperature in shunt circuit

The HOTCCC compensation circuit (MC5-MC24) generates two opposite piecewise linear currents in the low temperature region and high temperature region, respectively. In the low temperature region, when current $I_{p1} > I_{p2}$, transistors MC23 and MC24 are turned ON and a negative-TC compensation current I_{NTC2} is formed. The negative-TC compensation current I_{NTC2} is formed by Transistor MC24 from the output terminal V_{REF}. This operation is similar to a positive-TC compensation current added to the output to correct the negative-TC voltage of the reference voltage in the low temperature region. The current in M38 can be expressed as

$$I_{M38} = I_{M40} + I_{NTC2} \tag{10}$$

Therefore, the reference voltage can be expressed as

$$\begin{aligned} V_{REF} &= V_g + \Delta V_{GS}\left(I_{NTC}\right) \\ &= V_g + \sqrt{\frac{2}{\mu C_{ox} S_{M38}}} \times \left(\sqrt{\frac{I_{M37}}{L1}} - \sqrt{L2 \times I_{M37} + I_{NTC2}} \right) \end{aligned} \tag{11}$$

where $L1=S_{M37}/S_{M38}$, $L2=S_{M40}/S_{M39}$.

In the high temperature region, when current $I_{q1} > I_{q2}$, transistors (MC12–MC15) are turned ON

and a positive-TC compensation current I_{NTC1} is formed. The positive-TC compensation current I_{NTC1} is formed by Transistor MC15 from the output terminal V_{REF}. This operation is similar to a negative-TC compensation current added to the output to correct the positive-TC voltage of the reference voltage in the high temperature region. The current in M13 can be expressed as

$$I_{M38} = I_{M40} + I_{NTC1} \tag{12}$$

Therefore, the reference voltage can be expressed as

$$\begin{aligned} V_{REF} &= V_g + \Delta V_{GS}\left(I_{NTC}\right) \\ &= V_g + \sqrt{\frac{2}{\mu C_{ox} S_{M38}}} \times \left(\sqrt{\frac{I_{M37}}{L1}} - \sqrt{L2 \times I_{M37} + I_{NTC1}} \right) \end{aligned} \tag{13}$$

In the medium temperature range, the voltage variation is low, and the proposed TC compensation circuit does not generate any current to the output reference voltage, and transistors (MC12–MC15 and (MC2–MC24) are turned OFF. The proposed reference voltage is expressed according to (9) in the medium temperature range.

4. Simulation Results

Post-layout simulation was conducted on the proposed voltage reference in 55nm CMOS technology. The layout of the proposed voltage reference is shown in Figure 5, and the active area is 270μm × 70μm. The maximum power consumption is 2μA at 2.5V.

Figure 6 shows the simulation of reference voltage as a function of temperature with and without the proposed TC compensation. The TC of the proposed circuit exhibits an 88.6% improvement, from 28.5 to 3.19 ppm/℃.

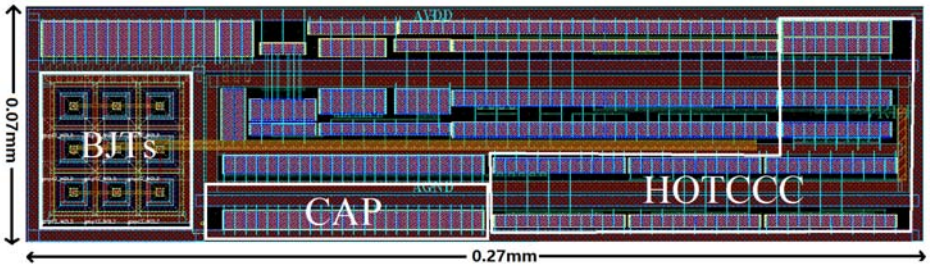

Figure 5. The layout of the proposed voltage reference

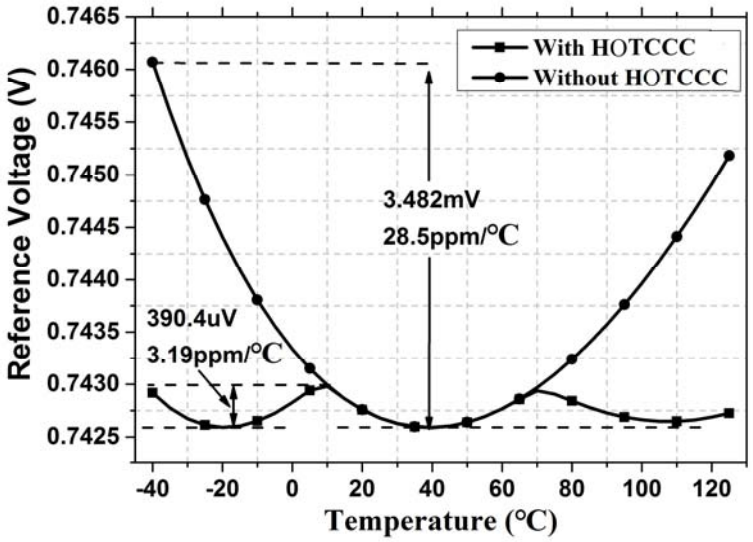

Figure 6. The reference voltage versus temperature with and without the HOTCCC.

The proposed reference achieves a PSRR of 82.45dB for frequencies below 1 KHz, and PSRR greater than 70 dB for frequencies below 10 KHz, as shown in Figure 7. The performance benefits from the design of cascade structure.

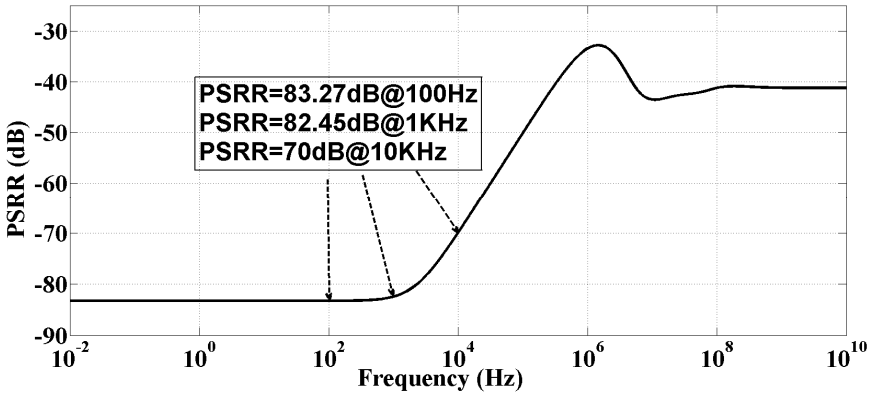

Figure 7. The result of PSRR simulation

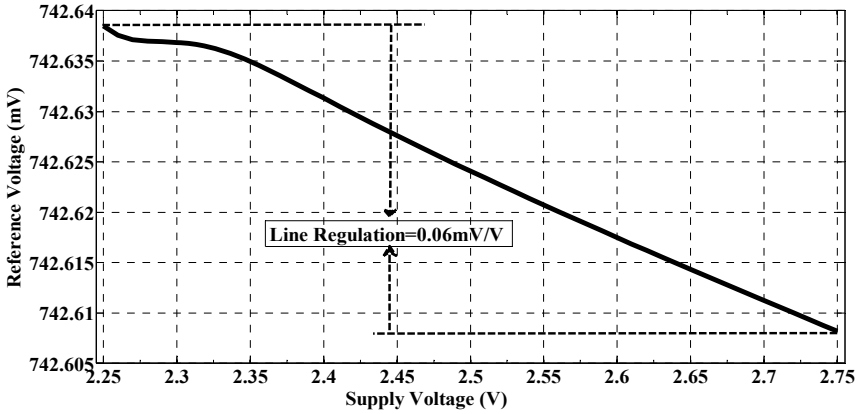

Figure 8. The supply dependence at room temperature.

The measured supply voltage dependence at 27℃is shown in Figure 8. The output voltage deviation of the proposed voltage reference is within 0.1 mV when the power supply voltage varies from 2.25V to 2.75V, and the linear regulation is about 0.06mV/V at room temperature.

5. Conclusions

In conclusion, this paper presents a precision reference simulated with a standard CMOS 55nm process. The simulation shows that the proposed TC compensation leads to an accurate reference voltage and a good TC over a wide temperature range. The designed positive-TC compensation and negative-TC compensation current can accurately correct the temperature drift. The best TC can approach 3.19ppm/℃ in a temperature range of −40℃ to 125 °C at 2.5 V. The output voltage is 742.6mV from a 2.25–2.75V at 27 °C. The maximum power consumption is 2μA at 2.5V. The active area is 0.019 mm2.

Acknowledgements

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