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Effects and methods of the BRL removal in solar cell

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Abstract: Boron diffusion is a conventional process in N-type silicon solar cells fabrication. The boron-rich layer (BRL) usually formed on the surface of silicon wafer in boron diffusion process, and the effective carrier lifetime can be sharply reduced by the BRL. In this paper, three methods were used to remove the BRL: high temperature nitric acid (HT-HNO_3) oxidation, chemical etching treatment (CET) and low temperature thermal oxidation (LTO). ECV and TEM are employed to characterized the dopant profiles and morphology of the silicon substrate surface after removing the BRL with different methods. Furthermore, the effective carrier lifetime of the samples is obtained by sinton instrument, and the reflectivity of the samples is measured. By analysis of the result date, we can conclude that the CET method can effectively remove the BRL and cause less carrier lifetime degradation comparing with other methods. What's more, the CET method have the most less influence on the doping profiles while removing the BRL. However, the CET method will cause a greater increase of the surface reflectivity than other methods.

1. Introduction

Czochralski (CZ) n-type silicon wafers have the advantages of less light induced degradtion, trace metal pollution effect during the preparation of N-type crystalline silicon solar cell, and the esponding lifetime is higher than the P-type silicon wafer. The minority carrier lifetime of passivated N-type silicon wafer can reached ms level[1-2]. At present, the two most commercialized solar cells, Panasonic HIT cells and Sun-power IBC cells with high photoelectric conversion efficiency are all based on N type silicon substrate[3-4].Therefore, the preparation process of N-type silicon-based solar cells has attracted widespread attention of researchers in recent years[5].

P-N junction is the core of solar cells. At present, there are three ways to prepare P-N junctions for N-type silicon substrate solar cells: Boron diffused junction, amorphous silicon / silicon hetero-junction and AL propulsion formed junction. The most widely used diffusion of the dopant is the diffusion of boron by the liquid source BBr3. As a liquid source, boron bromide is usually carried into the quartz tube of the diffusion furnace by nitrogen, and BSG is formed by the reaction of boron oxide with the surface of silicon at high temperature. However, in boron diffusion process, it is difficult to avoid the formation of a thin layer of the boron-rich layer (BRL). In this layer the B atom has no activity, and it will cause the structural defects, so the BRL has a serious impact on the wafer minority carrier lifetime. Therefore, it is important to remove the BRL from the diffused silicon wafer. There are three methods to remove the BRL at present:

(1) High temperature nitric acid (HT-HNO_3) oxidation: in this process, the BRL is oxidized by the high temperature nitric acid forming a borosilicate glass (BSG), then 2% HF is used to remove the BSG in order to achieve the purpose of the removal of a BRL.

(2) Low temperature thermal oxidation (LTO): the diffusion of the silicon wafer after 2% HF cleaning, remove the surface of BSG, and then in the diffusion furnace, oxidation of the BRL is performed at 600℃ for, and then through the 2% HF cleaning，the BRL can be removed.

(3) Chemical etching treatment (CET) uses a mixture of chemical oxidant and HF to remove the BRL. Firstly, the oxidant oxidized the B atoms to B_2O_3, and then 2% HF is used to removed the B_2O_3 (HF:CH3COOH:HNO3=1:100:100, etch 60s).

In this paper, the effect and advantage of using chemical etching to remove the BRL are investigated. The etching solution used in this experiment is a low concentration HF/HNO3/CH3COOH mixed solution.

2 .Experimental procedure

In this experiment, N-type CZ silicon wafers with <100> orientation, thickness of 180μm and resistivity of 1-3Ωcm were used. After cleaned by Radio Corporation of America (RCA), texturing is performed with TMAH/IPA alkaline solution. Then boron diffusion process formed a surface sheet resistance of 30Ω/□, and then, 2% HF is used to remove the BSG. Then different methods is used to remove the BRL[6]. After the removal of the BRL by chemical etching, the porous silicon is removed by using 1% NaOH solution for about 20s, so that the sheet resistance increases to about 60Ω/□.After that, AL_2O_3 is used on both sides of the silicon wafers to passivate the substrate surface. [7,8,9]. The control group was prepared by LTO and HT-HNO_3, and compared with chemical etching . Subsequently, a series of tests and characterization of B atom concentration, distribution profiles, minority carrier lifetime were carried out. The surface and cross-sectional of the BRL were examined using scanning electron microscopy (SEM) and transmission electron microscopy (TEM).

3 Results and Discussion

3.1 B atoms concentration analysis

After boron diffusion, the sheet resistance and doping profiles were characterized by electrochemical capacitance voltage (ECV) and the boron concentrations near the surface of substrate shown in Fig.1 by the black line is higher than the solubility of boron in silicon[7]. It is considered that the BRL has been formed in this diffusion depth. CET for the BRL removal, had a significant impact on the carrier lifetime in silicon solar cells. This experiment adopts three methods to remove the BRL, then ECV measurements were carried on the treated silicon wafer and the ECV results is shown in Fig. 1, the result of CET was shown in the pink line and LTO in the red line. As can be seen from the figure , the concentration of B atoms in the etched and post oxidized silicon wafer surface is reduced, which proves that the CET method had successfully removed the BRL[8].

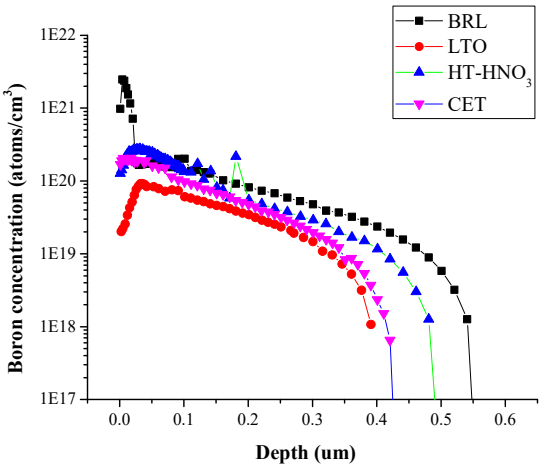

Fig.1 Boron doping profiles before and after removal of the BRL by different methods.

3.2 minority carrier lifetime and open circuit voltage analysis

The effective minority carrier lifetime, that is given by equation (1) is a measurement of the total carrier lifetime of the sample and it is approximately equivalent to the carrier lifetime at the surface with the inverse of the bulk lifetime been neglected.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{sur}} + \frac{1}{\tau_{bulk}} \quad (1)$$

Where τ_{eff} is effective minortity carrier lifetime, τ_{sur} is the surface carrier lifetime and τ_{bulk} is the bulk carrier lifetime.

The structure of N-type crystalline silicon wafers solar cell was shown in Fig.2. Both sides diffusions were used and the measurements are performed after removal of BSG using 2% HF, and the emitter prepared by the diffusion of both sides were retained.

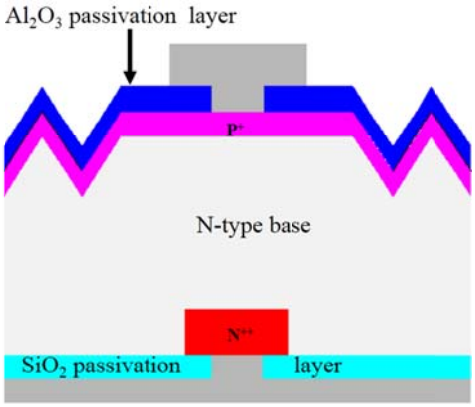

Fig.2 Schematic cross section of solar cells measured in this experimentation

AL_2O_3 layers showed the best passivation effect for p-type emitters and so a thickness of 80nm AL_2O_3 layer is used to passivate the BRL removed emitter. AL_2O_3 passivation can improve the cattier lifetime by almost 10 times compared to the bare wafers [9].

The minority carrier lifetime values, with or without BRL, were measured in Sinton lifetime measurement instrument. The lifetime test results was shown in Fig.3, the carrier lifetime of the wafer with BSG removed is 459.72μs, the average lifetime after removing the BRL silicon wafer by HT-HNO_3 was 361.35μs, the average lifetime after removing the BRL by LTO is 255.31μs , the lifetime measured after removing the BRL by CET is 880.76μs. By contrast test, the minority carrier lifetime obtained by CET method is obviously higher than the other two methods, so the CET can effectively remove the BRL and improve the minority carrier lifetime.

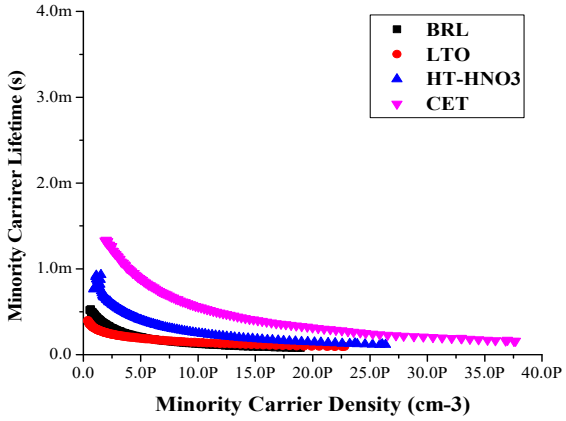

Fig.3 Minority carrier lifetime of the wafer by different processing;

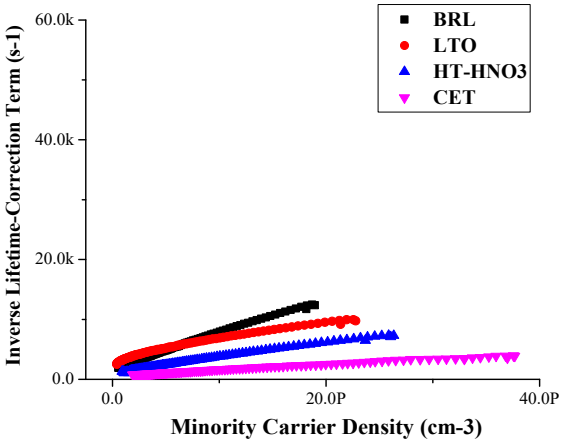

Fig.4 Inverse Lifetime-Correction Term of the wafer by different processing;

Moreover, the open circuit voltage (Voc) and the emitter saturation current density (Joe) was measured after removing the BRL. As shown in Fig.4, Voc increase from 620mv to 635mv after removing the BRL. To a certain extent, Voc reflects the complex situation of silicon and had a great influence on the real Voc. At the same time, Joe decreased from 240fA / (cm^2) to 40fA / (cm^2) after removing the BRL. It was also found that the removal of the BRL greatly reduced the recombination of minority carriers and therefore improving the lifetime of minority carriers. [9,10]

3.3 reflectivity analysis

Chemical methods are destructive to the surface morphology of silicon wafers, especially the CET system, which can directly corrode silicon. Therefore, it is necessary to consider the influence on the textured silicon wafer surface by CET system. So we tested the reflectivity of the silicon wafer before and after etching. The range of the wavelength range changed from 300nm to 1100nm. As shown in Fig. 5, the reflectivity increased from 15.6% to 19.5% without the using of the antireflection film. It shows that the CET system had slight influence on the light trapping structure of silicon wafer.A slight increase in reflectivity could be seen, but in the end of the process while Al2O3 antireflective film was coated, the reflectance increased seldomly, and mainly concentrated in the long wavelength region, and the influence on the final cell efficiency was basically negligible. [8,9]

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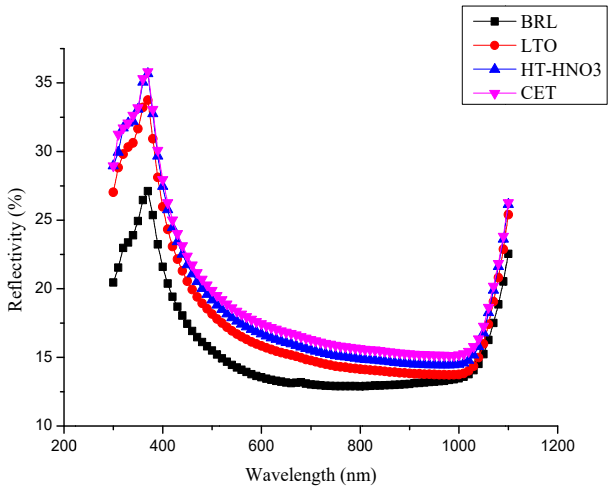

Fig.5 Front reflection spectra of wafers before and after wet-chemical etching

Corrosion does not have a significant effect of light trapping effect. we analyzed SEM results before and after corrosion of silicon wafer surface, as shown in Fig.6, light structure without wafer surface damage caused by the chemical etching can keep the surface of solar cell surface in Pyramid[11,12].

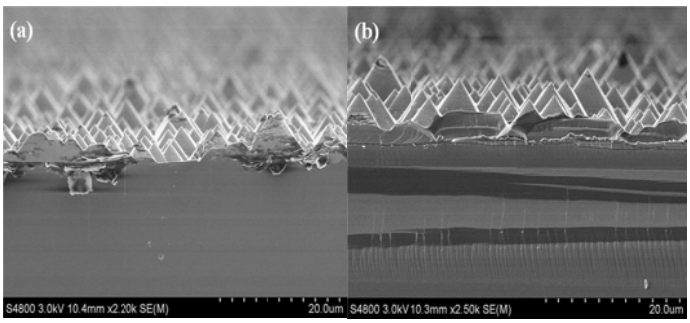

Fig.6 SEM micrographs of wafers，surface：（ａ）after chemical etching treatment；（ｂ）before chemical etching treatment；

Furthermore, in order to exam that whether BRL is removed, TEM of silicon wafer surface before and after corrosion was analyzed, as shown in Fig.7, chemical corrosion of the silicon surface can effectively removed the BRL. [11]

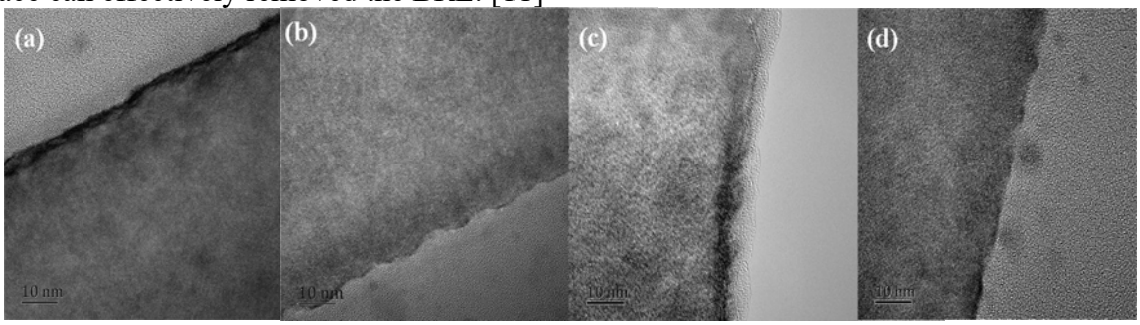

Fig.7 TEM micrographs of wafers，surface：(a) with BRL；(b) by CET；(c) by LTO; (d) by HT- HNO_3;

4. Conclusion

In summary, three methods were used to remove the BRL formed in boron diffusion process. ECV, TEM and lifetime test confirmed that the CET can successfully remove the BRL and improve

the minority carrier lifetime and Implied-Voc at the same time reducing the emitter saturation current density. Compared with LTO and HT-HNO_3, this process can obviously reduce the process time and high temperature time. And through the analysis of the surface morphology and reflectivity before and after corrosion, it is considered that the removal of the BRL by chemical etching will not affect the light trapping effect of silicon wafers.

Acknowledgments

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