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A Method to Determine the Synthetical Acceleration Factor of Electronic Equipment Based on Failure Physics

Haoping Yan[1,*], Yuqing Hu[2], Yuexuan Ma[1] and Tao Wang[1]
[1]China Aero-Polytechnology Establishment, CAPE, Beijing 100028, China
[2] School of Reliability and Systems Engineering, Beihang University, Beijing 100191, China
[*]Corresponding author

Abstract—**Accelerated test is commonly used to obtain reliability data of products by exerting loads over usage conditions for highly reliable and long life products, and it's very significant to decide the acceleration factor (AF) in the test. For electronic equipment, the AF obtained by traditional method can only consider the internal failures caused by the components, without covering the interconnection failures caused by solder joints, pin failures, etc. Thus, a new method based on failure physics is presented in this study to determine the synthetical AF taking both internal failures and interconnection failures into consideration. The AF of the internal failures caused by the components is calculated based on the Arrhenius model, and the AF of the interconnection failures caused by solder joints is captured by reliability simulation test with a software called Calce PWA. Then, the synthetical AF of the electronic equipment can be determined by weighted fusion of both two AFs. Finally, the feasibility and validity of the proposed method can be verified by an application of an embedded electronic device.**

Keywords-component; reliability test simulation; accelerated test; acceleration factor

I. INTRODUCTION

With the rapid development of science and technology, modern products have been more and more reliability, especially for electronic equipment. The mean time to failure (MTTF) of electronic products has reached thousands of hours. Thus, traditional reliability test under the usage condition cannot validate the reliability index within an acceptable time and accelerated test is developed. Accelerated test is commonly used to obtain the reliability data of products over a short time period, to help extrapolate life and reliability under usage conditions [1]. In an accelerated test, products are exposed to high-than-use conditions to get reliability data in a short time [2][3].

In an accelerated test, the acceleration factor (AF) refers to as the ratio between the life-time under the accelerated stress level and that under the usage stress level, which can reflect the effect of a certain accelerated stress level [4]. In the last decade, there are many publications studying the methods of determining the acceleration factors [5][6]. However, for electronic equipment, the AF obtained by traditional method can only consider the internal failures caused by the components, without covering the interconnection failures caused by solder joints, pin failures, etc. Thus, a new method based on failure physics is presented in this study to determine the synthetical AF taking both internal failures and interconnection failures into consideration. The internal failures caused by the components can be calculated based on the Arrhenius model, and the interconnection failures caused by solder joints can be captured by reliability simulation test with a software called Calce PWA. Then, the synthetical AF of the electronic equipment can be determined by the weighted fusion of both two AFs.

The remaining paper is organized as follows. In section 2, reliability simulation test based on failure physics is presented. In section 3, the method to determine the synthetical AF of electronic equipment based on failure physics is proposed. In section 4, the feasibility and validity of the proposed method can be verified by an embedded electronic device. Section 5 concludes this paper.

II. RELIABILITY SIMULATION TEST BASED ON FAILURE PHYSICS

The AF of interconnection failures caused by solder joints can be captured by reliability simulation test with a software called Calce PWA. The main procedures of reliability simulation test include information collection, digital prototype modeling, stress analysis, reliability prediction and reliability evaluation. The flow chart of the reliability simulation test is shown in Figure 1.

Firstly, we collect the products information including the CAD models, the material properties of component and the material size of each component. Then, the FEA models for vibration analysis and CFD models for thermal analysis can be established respectively. Under the practical operating conditions and the environmental conditions in the product life cycle (i.e. test profile), the vibration analysis and thermal analysis could be conducted. Finally, reliability evaluation will be outputted based on the results of vibration analysis, thermal analysis and the relevant failure physics model with the software Calce PWA.

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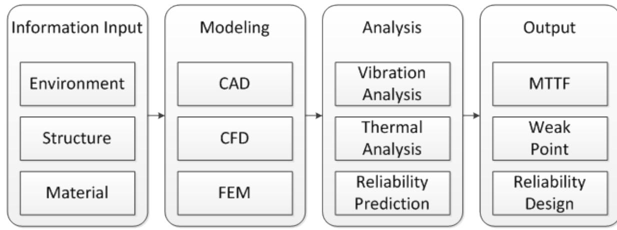

FIGURE I.THE PROCEDURES OF RELIABILITY SIMULATION TEST BASED ON FAILURE PHYSICS

A. Thermal Analysis

Thermal analysis can be conducted by the engineering finite element analysis software Flotherm. By setting the material properties and structural characteristics of the equipment, and loading the corresponding temperature stress, the temperature distribution cloud, temperature gradient, the temperature of components on the PCB can be obtained. Thermal analysis can be used to expose potential thermal problems and optimize thermal design to improve the reliability of the equipment. In addition, the results of thermal analysis will be an input of the reliability prediction.

B. Vibration Analysis

Vibration analysis is carried out on the mechanical structure of the product by the software Ansys. Based on the CAD model of the product and the corresponding information such as the size, material properties, volume and mass distribution of the parts, the vibration load model is established by using the finite element analysis method. Then, the modal analysis and random vibration response for the components of the product can be conducted. Besides, the vibration analysis result is another input of the reliability prediction.

C. Reliability Prediction

The reliability prediction is based on failure physics using the software Calce PWA. The results of thermal analysis and vibration analysis are taken as the inputs of the failure mechanism model. Other parameters of the model are set according to the product characteristics. By reliability analysis, the weak point of the equipment and the prediction of life time of the equipment can be obtained. The reliability prediction method is based on stress damage analysis and accumulation damage analysis. Stress damage analysis is a reliability analysis method that studies the possible failures modes, failures mechanisms of each components and the impact of the various failures modes on the specific requirements for other components. Damage accumulation analysis is generally for products with the loss failure mechanism, and the failure occurs when the losses of the materials accumulate to a certain threshold.

III. DETERMINATION OF SYNTHETICAL AF BASED ON FAILURE PHYSICS

A. AF of Interconnection Failures Based on Reliability Test Simulation

The AF of interconnection failures is caused by failures of solder joint and pin under the temperature cycle and vibration stress. The life-time under the normal stress T_U and that under accelerated stress level T_A of the electronic equipment can be calculated by the reliability simulation analysis introduced in section Ⅱ. Then, the AF of interconnection failures a_1 can be obtained as,

$$a_1 = \frac{T_U}{T_A} \tag{1}$$

B. AF of Internal Failures Based on Arrhenius Model

The AF of internal failures caused by the components of the electronic equipment can be obtained based on the Arrhenius model. The Arrhenius model focuses on the effect of reliability under *a* certain temperature for electronic equipment, which can be expressed as,

$$r = A\exp\left(-\frac{E_a}{kT}\right) \tag{2}$$

where r denotes the reaction rate, A denotes a temperature-independent unknown constant, and Ea denotes the activation energy. Different products characterized different activation energy. Generally, the activation energy is between 0.3eV~1.2eV, which is set as 0.79 in this paper according to the relevant criterion. k is the Boltzmann constant, which is 8.617385×10-5eV/K. T is the Kelvin temperature (K). According to the Arrhenius model, the acceleration factor a can be calculated as,

$$a = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T_1}\right)\right] \tag{3}$$

where T_0 is the usage stress level and T_1 is the accelerated stress level for electronic equipment. Then, the acceleration factor of the internal failures a_2 can be calculated based on the test profile and the Arrhenius model.

C. Method of Obtaining The Acceleration Factor

Finally, the two factors are merged to obtain the synthetical AF considering both internal failures of the components and interconnection failures of the electronic equipment. According to the historical failure data, the ratio of interconnection failures and internal failures could be obtained as λ_1:λ_2. Then the synthetical AF a_T can be obtained by weighted fusion of the two AFs expressed as,

$$a_T = a_1\lambda_1 + a_2\lambda_2 \quad (4)$$

IV. Numerical Example

To verify the proposed method, we calculate the AF of an embedded electronic equipment for the corresponding acceleration profile. The device consists of a PCI card (including a shell structure and a Printed Circuit Board (PCB)) and a port adapter (including a shell structure and a PCB), and the two are connected through a cable, as shown in Figure 2.

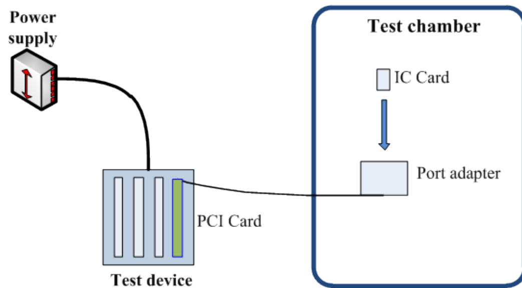

FIGURE II. EMBEDDED ELECTRONIC EQUIPMENT DIAGRAM

A. Test Profile

1) Usage test profile

The proposed equipment is a ground fixed equipment. According to the typical integrated environmental test profile of ground fixed equipment in 'GJB899A-2009 Appendix B', environmental profile can be selected. The task test profile is determined as 'text encryption and decryption and self-test'. Taking into account the actual usage conditions of the equipment, the combined environmental usage test profile is adopted as shown in Figure 3.

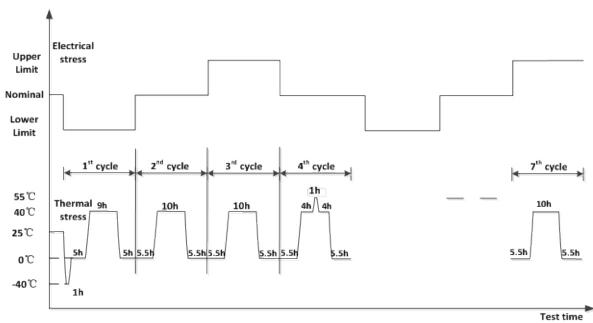

FIGURE III. THE COMBINED ENVIRONMENTAL USAGE TEST PROFILE FOR 168 HOURS

a) Electrical stress

(1) Electrical stress includes the power on/off cycle, operation cycle and voltage changes. Apply the nominal voltage to 50% of the turn-on time, and apply the upper and lower voltage to 25% of the turn-on time.

(2) Change the electrical stress at the beginning of each operation cycle, i.e., the first and fifth operation cycle are the lower limit voltage, the second, fourth and sixth operation cycle are the nominal voltage, and the third and seventh operation cycle are the upper limit voltage.

(3) The duration of each cycle is 21-22 hours.

(4) Electrical stress: 4.5V to 5.5V.

b) Thermal stress

The temperature stress level reflects the actual environment during the usage conditions. The thermal stress of each operation cycle consists of two stages. For the sake of calculation, cold dip and hot dip alternate in different operation cycles, and the details are described as follows:

(1) The thermal stress reflects the actual environment during the usage condition. Thus, the thermal stress level is determined as the operation temperature. The cold dip is loaded in the first operation cycle for an hour, and the hot dip is loaded in fourth operation cycle for an hour. The thermal stress levels loaded in the 2nd, 3rd, 5th, 6th operation cycles vary within the range of operation temperature.

(2) The cold dip is loaded in the first cycle. When the temperature has been cooled to cold dip temperature, the condition of cold dip should be kept for 1 hour. Then, the temperature need to be heated to low operation temperature and be kept for 5 hours. Reheat the test temperature to high operation temperature and keep it for 9 hours. Finally, the cycle is ended with the operation temperature for 5 hours.

(3) For the fourth cycle, the test temperature is kept at low operation temperature for 5.5 hours, and then raised to the high operation temperature and kept for 4 hours. Then, the hot dip is loaded for an hour, when the temperature is raised to the hot-dip temperature. After that, keep the high operation temperature for 6 hours, cool again to the low operation temperature and keep it for 5.5 hours.

(4) For the 2nd, 3rd, 4th, 6th, 7th cycles, the test temperature is kept at low operation temperature for 5.5 hours, then heated to the high operation temperature, and kept for 10 hours. Then the cycle is ended with the low operation temperature for 5.5 hours.

(5) Thermal stress level: the operation temperature is 0°C to 40°C, and the storage temperature is -40°C to 55°C.

c) Humidity stress

Humidity stress will be loaded during the inactive hot-dip condition, and the humidity is maintained at 75% to 95%.

d) Vibration stress

(1) The vibration stress is loaded for twice, one is loaded before the first cycle and the other is loaded after the last cycle.

(2) Neither thermal stress nor electrical stress are loaded in the vibration stress test.

(3) The frequency of the vibration stress is selected as an optional non-resonant frequency within the range of 20Hz-60Hz, and the direction is vertical. For sinusoidal vibration test, the corresponding amplitude is $22m/s^2$ and duration is 20min.

2) Accelerated test profile

For the accelerated test, the electrical stress, humidity stress and vibration stress remain the same with the usage test profile .However, for the thermal stress, the high stress level is adjusted as 60°C and low stress level is 0°C. Besides, the ratio of the time for the high stress level and the low stress level is 7:1. The rate for the heating process is kept at 3°C /min, and that is kept at -3°C /min during the cooling process. The corresponding accelerated profile is shown as Figure 4.

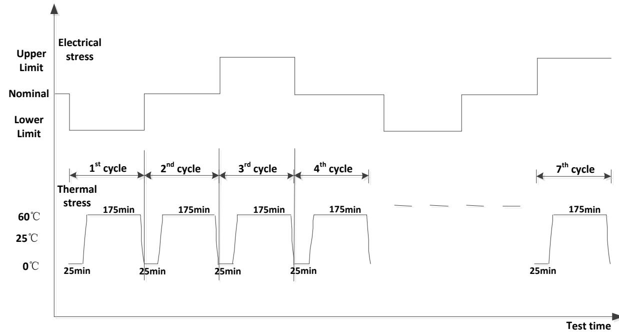

FIGURE IV. ACCELERATED INTEGRATED ENVIRONMENTAL STRESS PROFILE

B. Test Profile Reliability Simulation Test Based on Failure Physics

Based on the information of thermal design, materials, components, etc., the reliability simulation tests for the PCI card and the PCB in the port adapter are adopted according to section III.A, respectively. Since the device is a ground fixed equipment, the failures caused by vibration could be ignored, and the simulation analysis only takes the thermal stress into account. Thermal analyses and reliability predictions for the two PCBs were conducted, and the corresponding temperature analysis cloud diagrams and PCB simulation models are shown in Figure 5 and Figure 6.

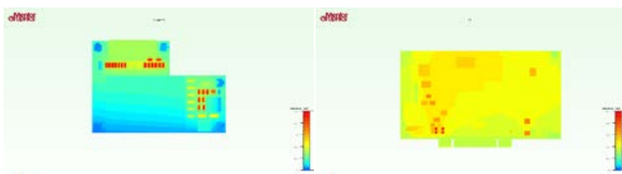

FIGURE V. CLOUD DIAGRAMS OF TEMPERATURE ANALYSIS

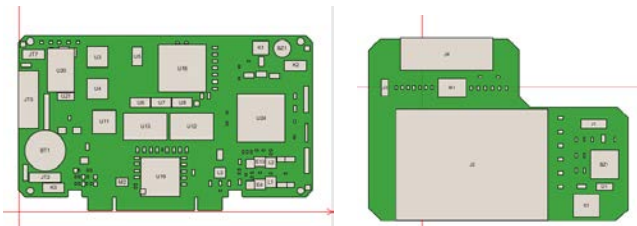

FIGURE VI. PCB SIMULATION MODELS

Based on the software Calce PWA, the MTTFs of the equipment under the usage test profile and accelerated test profile can be calculated, and the corresponding results are shown in Table 1 and Table 2,

TABLE I. MTTF UNDER USAGE TEST PROFILE

No.	Name	Types of distribution	MTTF(h)
1	Device	Weibull distribution	184110.04
2	Adaptor	Weibull distribution	493269.95
3	PCI	Weibull distribution	192384.58

TABLE II. MTTF UNDER ACCELERATED TEST PROFILE

No.	Name	Types of distribution	MTTF(h)
1	Device	Weibull distribution	16249.53
2	Adaptor	Weibull distribution	91860.86
3	PCI	Weibull distribution	16310.75

C. Figures and Tables Determination of the synthetical AF

1) Determination of interconnection AF

As shown in Table 1 and Table 2, the T_U under usage test profile is 184110.04, and the T_A under accelerated test profile is 16249.53. Thus, the interconnection AF is,

$$a_1 = \frac{T_U}{T_A} = \frac{184110.04}{16249.53} = 11.33 \tag{5}$$

2) Determination of internal AF

In the Arrhenius model, generally activation energy is selected as 0.79 and k is 8.617385×10-5eV/ K. In order to effectively calculate the AF caused by the internal failures of the device, the AFs of each stress level under the test profiles are calculated compared to 0°C based on (3), and then the AFs under the usage test profile and the accelerated test profile could be obtained by average as shown in Table 3 and Table 4.

TABLE III. MTTF UNDER USAGE TEST PROFILE

Test spectrum	Lasting time (h)	Temperature in profile	AF
Low temperature	11	0	1.00
High temperature	10	40	73.09
Whole profile	21	--	35.30

TABLE IV. MTTF UNDER ACCELERATED TEST PROFILE

Test spectrum	Lasting time (h)	Temperature in profile	AF
Low temperature	25	0	1.00
Process	40	30	27.80
High temperature	175	60	424.47
Whole profile	240	--	314.20

Thus, the internal AF is,

$$a_2 = 314.2 \div 35.3 = 8.9 \tag{6}$$

3) Synthetical AF

According to the historical failures data of the electrical equipment, the proportion of interconnection and internal is about 2:8, hence the interconnection coefficient λ_1 is 0.2, and the internal coefficient λ_2 is 0.8. Finally, according to (4) the synthetical AF could be calculated as,

$$a_T = 0.2 \times 11.33 \ + 0.8 \times 8.9 = 9.4 \tag{7}$$

V. CONCLUSIONS

In this study, a new method based on failure physics is presented to determine the synthetical AF taking both internal failures and interconnection failures into consideration. The AF of internal failures caused by the components is calculated based on the Arrhenius model, and the AF of interconnection failures caused by solder joints is captured by reliability simulation test with a software called Calce PWA. The synthetical AF is determined by weighted fusion of both two AFs. Also, the feasibility and validity of the proposed method are verified by an application of an embedded electronic device. Besides, the proposed method could play an important role on reliability screening, reliability test design and so on.

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