Design of Four-rotary-wing Aircraft Targeting System

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Abstract. In order to achieve the design of visual art quad -rotor aircraft targeting system, we have, by combining design principles of image processing system and Bluetooth communication, rendered the design method of four-rotary-wing Aircraft Targeting System on the basis of the latest technology of programmable system on chip (SOPC). The method, which is innovative and relevant , has initially achieved four –rotary-wing aircraft's intelligentization and specific object targeting.

Introduction

Four-rotary-wing aircraft is an unmanned aerial vehicle, which, jointly driven by four rotary wings, takes off and lands vertically. With new and simple structure, it's easy to control, and can take off at a high speed, fly smoothly and be easily suspended in the air. Therefore, it enjoys a broad prospect of application in detection and investigation. FPGA-based Nios II multi-core processor system, with such features as flexible design, hardware and software programming and rich IP core library support, has brought greater flexibility to the design of modern electronic products. As a hot topic in intelligentization, enhancing the intelligent level of four-rotary-wing aircrafts is of great significance to our life and production.

Nios II FPGA-based multi-core processors in this article, by using visual technology and Bluetooth communication methods, have achieved the design and framework of the four-rotary-wing aircrafts' intelligent control and positioning of specific objects.

The Design of Hardware Layer

This article describes an Image Recognition System that is designed on SOPC Nios II-based system. The system uses SDRAM Memory as the image data buffer and SD Card as a Nios II program memory and data memory. The reading and writing of SDRAM needs to be done by the SDRAM Controller. The design of Image Recognition System uses a 4-port SDRAM Controller based on FPGA. [1]In order to let Nios II have access to SDRAM directly, we need to use SDRAM Controller based on the Avalon Bus. Since these two SDRAM Controller cannot coexist, we have designed a Data Acquisition Controller based on Avalon Bus Peripherals. Nios II takes advantage of the Controller to control the Data Acquisition Module directly, and thus we indirectly have access to the SDRAM's content, read the data and send it to SD Card, and carry out further processing.

The picture of hardware physical things are as follows:

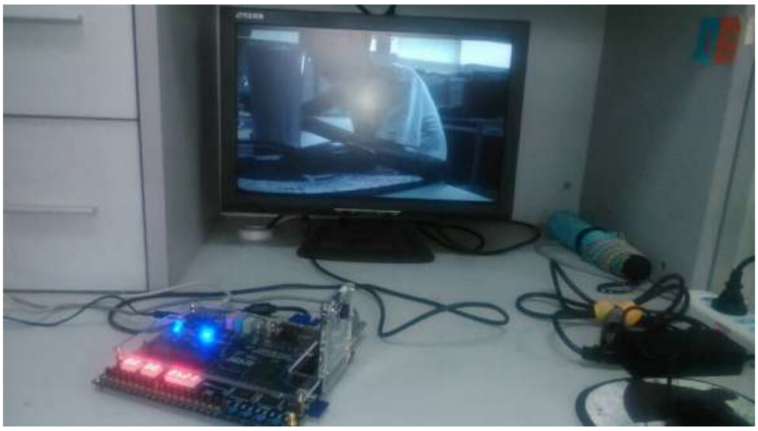

Fig. 1 Physical things of hardware

The design of the hardware layer has been completed with reference to the "DE2-70 CAMERA" of user reference samples provided by Altera Company, Its RTL-level circuit design is shown in fig 2

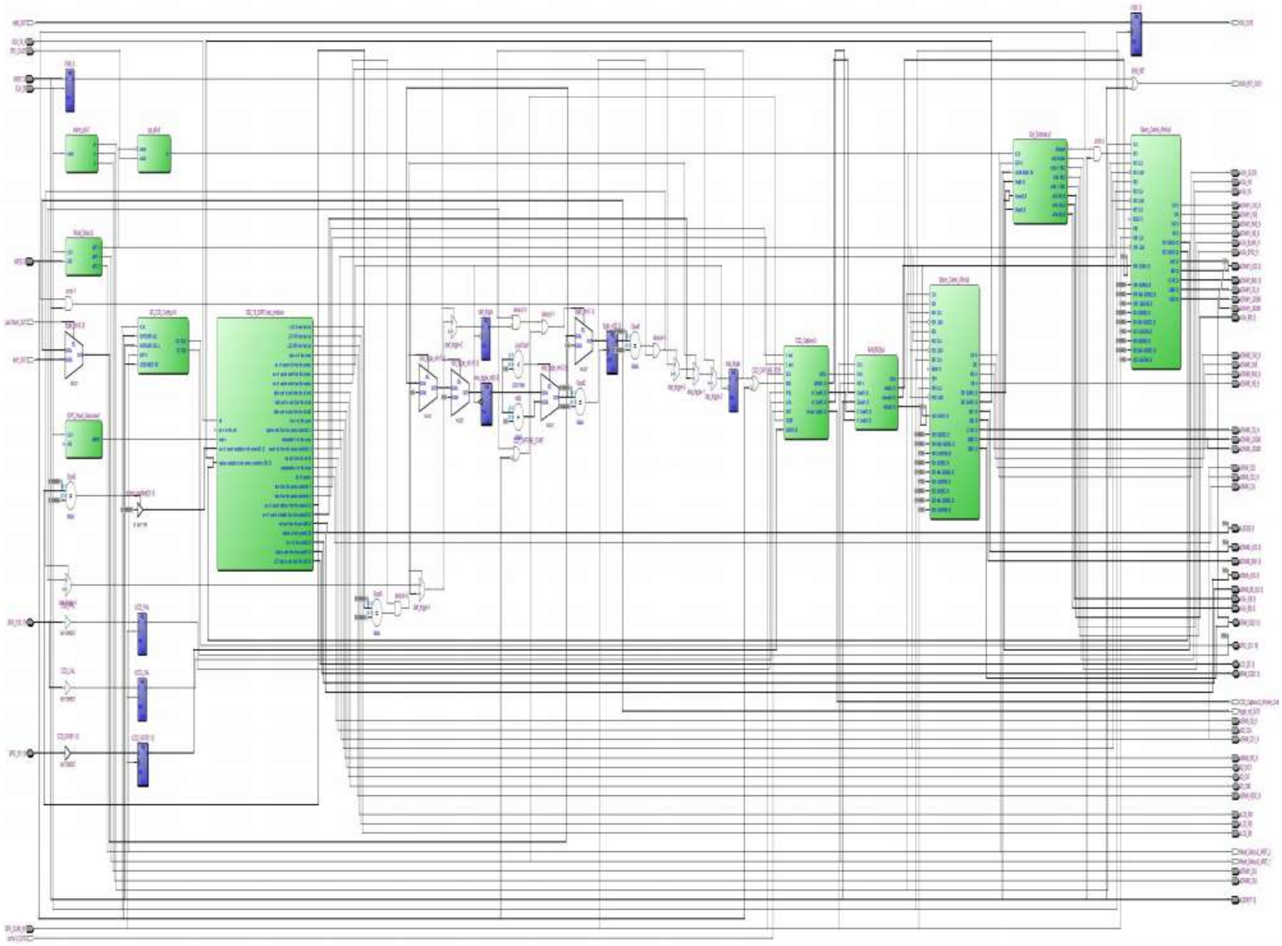

Fig. 2 RTL-level circuit design system architecture

Top module defines input and output variables which are associated with FPGA pins, and connects the various sub-modules with the Wire Bus and the Reg Bus. Because of too many top-level module input and output variables, in order to avoid the body to say, here is no longer listed. The descriptions of associated pins and program blocks can be got in each module pin descriptions.

The functions of each module and associates between them in the top-level module are as follows: [2]I^2C Configurator can define exposure and other parameters on the CMOS Camera with the

I^2C Agreement; Data Acquisition Module can get the image data from the photos captured by camera, and send the data to the Format Conversion Module; Format Conversion Module Data into RGB format, and then sent through a multi-port SDRAM Memory Controller; Format Conversion Module change the data into RGB format, and then sent them to SDRAM through a multi-port SDRAM Memory Controller; When the LCD Controller sends a signal to the reading FIFO1 of SDRAM Controller, the image data can be read out through the SDRAM Controller and be sent to the LCD to display(In order to debug we use the LCD to display image information, the image data will not display in the end, which means that LCD Controller won't be needed); When the LCD Controller sends a signal to the reading FIFO2 of SDRAM Controller, the image data can be read out through the SDRAM Controller and be sent to SD card for data processing such as Image Recognition with C program. I^2C Configurator, Data Acquisition Module, the Format Conversion Module, SDRAM Controller, LCD Controller are FPGA hardware implementation. The Nios II, Avalon Bus, SPI Controller, Data Acquisition Controller constitute SOPC system, also embedded in the FPGA. [3] Nios II can use SPI Controller to deal with data on the SD Card. SOPC Builder also comes with SDRAM Controller for the access to the Nios II SDRAM Memory, but because a multi-port SDRAM Controller has been used in the system, therefore the SDRAM Controller based on the Avalon Bus cannot be used. [4] To solve the problem that Nios II having access to SDRAM, we designed the Data Acquisition Controller based on Avalon Bus. The Nios II have the access to SDRAM through Data Acquisition Controller.

Nios II Soft-Core Building.

The Nios II Cpu designed in this article consists of the following parts:

Cpu Module, image information related calculations.

Onchip_mem Module and Ssram Module, Storing image information and the corresponding results.

sd_clk,sd_dat,sd_dat3,sd_cmd, the SD card control.

Uart Module, bluetooth module for implementing additional information and FPGA communication.

Tristate_bridge Module, connecting the individual modules.

Camera_controllor_0 Module, controlling the camera to collect data.

Due to space restrictions, a detailed description of SOPC Builder and used in this article doesn't go into details. Soft Core eventually constructed is shown in Fig 3:

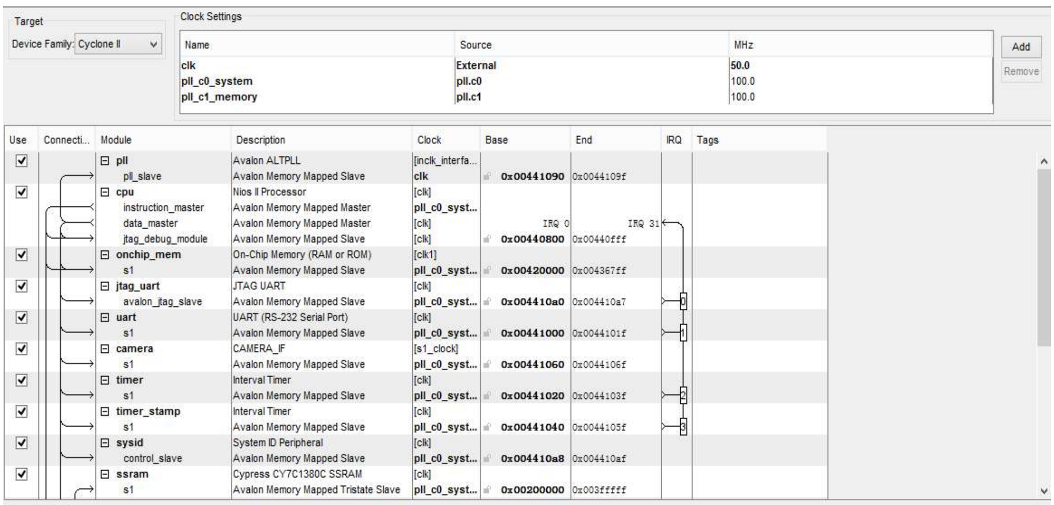

Fig 3. SOPC soft-core design

The Design of Software Layer

The hardware layer can be connected to the software layer through soft-core processors. Besides, we can control the hardware by utilizing the mapping interface of hardware layer.

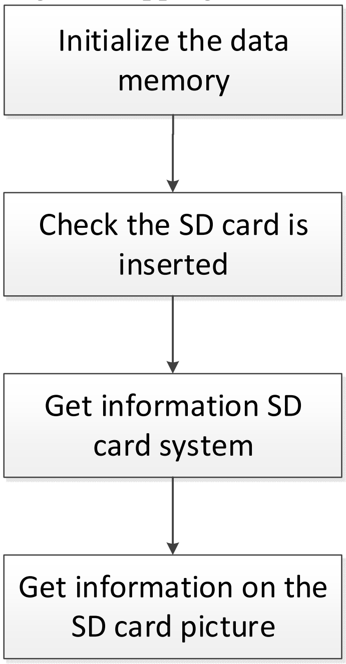

Fig 4. SD card reader processing flow

The processing flow consists of three nested layers. The bottom layer refers to the SD Card driver, the middle a file manager, and the upper put the other two parts together to complete SD Card reading.

The result of the program is shown below (Fig 5):

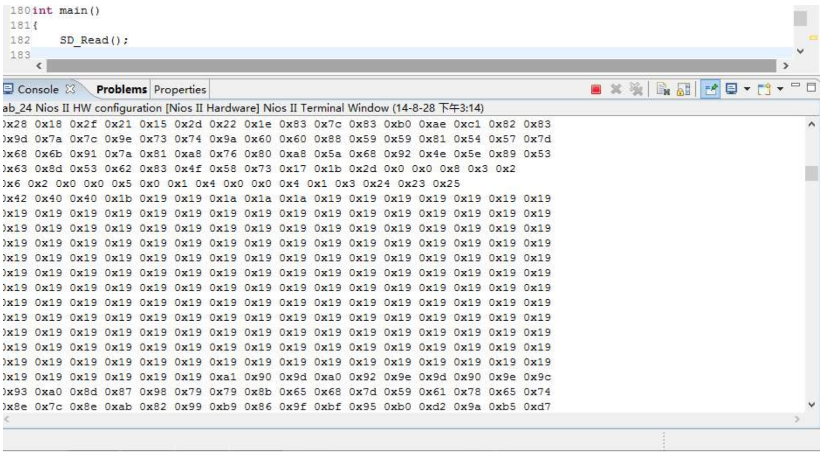

Fig 5. SD card information reading results

Reading Operations of the Data Acquisition Controller.

From the mapping software layer of Data Acquisition Controller ("system.h"), we can see its physical address

(CAMERA_CONTROLLOR_0_BASE) is 0x00000000.

From the parameter definitions of Data Acquisition Controller [5] we know base register address: Offset = 0x00, the registers of controlling the camera data acquisition can be set "1"(active) or "0"(inactive), its function is used:

IOWR (CAMERA_CONTROllOR_0_BASE, 0x00,0 / 1) [6];

Offset = 0x01, the register of controlling camera data collection received can be set "1"(active) or "0"(inactive), its function is used:

IOWR (CAMERA_CONTROllOR_0_BASE, 0x01, 0 / 1);

Offset = 0x10, this address will get the data of SDRAM memory captured by the camera. We need to debug errors through LCD, but also need to collect image data from the same address. To solve this problem, we use an external button SW [9] to assign reading permissions. If it is set "1", it means that the LCD reads data. If it is set "0", it means that the data collection controller can read data. Its function is as follows:

IOWR (CAMERA_CONTROllOR_0_BASE, 0x10) [7].

According to the 3 functions, the image information can be obtained from the hardware layer for further processing.

The results are as follows (Fig 6):

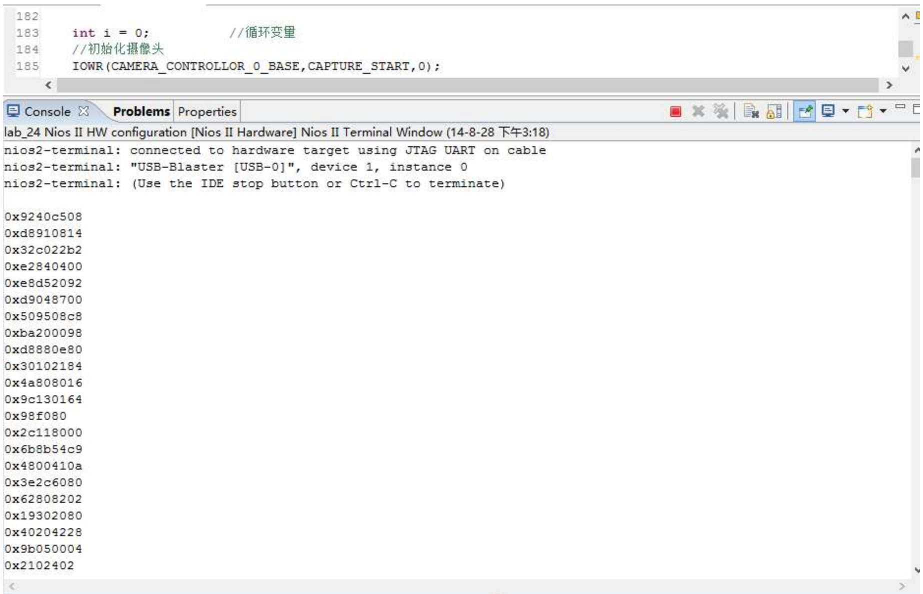

Fig. 6 results of camera information reading

The Design of Aircraft

Four-rotor-aircraft uses four brushless motors to pitch,roll and yaw. In order to make up the insufficiency of Obstacle avoidance function of the Flying Control Board, the design uses FPGA as Auxiliary arithmetic units. The deigned system is controlled by both FPGA and MWC Flying Controlling Board [8]. It collects sonar sensor data and sends serial data to the Flying Controlling Board through FPGA. According to the experiment, we can solve the problem of data reading and transmission by Using FPGA and MWC dual core processor in a better way, which makes the control more efficient.

Four-rotor-aircraft depends on MWC which can read the data from three axis accelerometer,gyro sensor,magnetic heading sensor and Pressure sensor. MWC calculates the data and obtain the attitude and altitude of four rotor aircraft, meanwhile, we can get the PWM signal which can control brushless motors by embedded control algorithm. As a consequence, the speed of four motors can be changed so that we can control the aircraft.

Its hardware system mainly includes MWC Flight Control Board and FPGA Board. MWC Flight Control Board is a kind of open source flight control board made by the foreign friends. There are MPU6050 and HMC5883L attitude transducer on the board [9]. FPGA is a kind of programmable logic array. We mainly use it to read data from sonar sensor to generate the control command. Then we can use the RS-232 port on FPGA and UART port on MWC to realize the asynchronous serial communication. At last, we can realize obstacle avoidance function or the ranging function in order to perfect the function of aircraft.

As is known to us, FPGA has a RS-232 asynchronous communication interface, meanwhile, MWC Flight Control Board has a UART interface [10]. When we use them, the only thing we need to do is to make a RS232 to TTL pin-board as a bridge. Firstly, we need to connect FPGA with the pin-board by nine direct serial line. Secondly, we should make sure that MWC and the pin-board are connected by dupont Line. In this way, we can realize the transmission of signals between FPGA and MWC.

Double processor system of MWC and FPGA can successfully solve the problem of acquisition and processing of sensor data, which can add more different sensor types to the flight. According to the experiment, the four-rotor-aircraft control system can realize the control in an efficient way, which makes the operation more accurate.

The flying aircraft is as follows:

Fig. 7 Flying aircraft

The Design of Communication Module

As for Bluetooth module, FPGA module has no Bluetooth module and interface. For this reason, we have decided to build one by using Verilog Language module at the hardware level. With the Verilog code finished, we have achieved the communication of Bluetooth Module.

We wrote a phone APP. APP for Android operating environment. Combined with the Bluetooth protocol, written procedures Android, finally connect the phone with a Bluetooth communication module. APP can make local phone pictures sent by mobile phone comes with Bluetooth to Bluetooth communication module. APP can also control the aircraft's flight by send digital signals to the Bluetooth communication module.

Flow chart which for set up a Bluetooth phone connection as follow (Fig. 8):

Bluetooth module is connected to FPGA board's serial portvia via USB to serial cable. Then the telephone's Bluetooth can be connected to the FPGA board's Bluetooth Communication Module. The telephone's Bluetooth search for the port number of the FPGA board's Bluetooth and connect with it.After the basis of communication is built up, we write corresponding code of Verilog. Then the code of Verilog will be embedded into the FPGA board as the underlying driver.The driver is be seen as a module of the FPGA board. When the phone is pressed different keys,the phone will produce different commands.The commands are transmistted to the FPGA board's Bluetooth through the telephone's Bluetooth.The FPGA board receives the commands to control the four-rotor aircraft's hovering, flying and other movements. In addition, the mobile phone sends the binary format image to the FPGA board's Bluetooth through its Bluetooth.After the FPGA board's Bluetooth receiving the image,the image can be sent to FPGA's image processing module for processing and matching and matching and matching results will be sent to your phone.

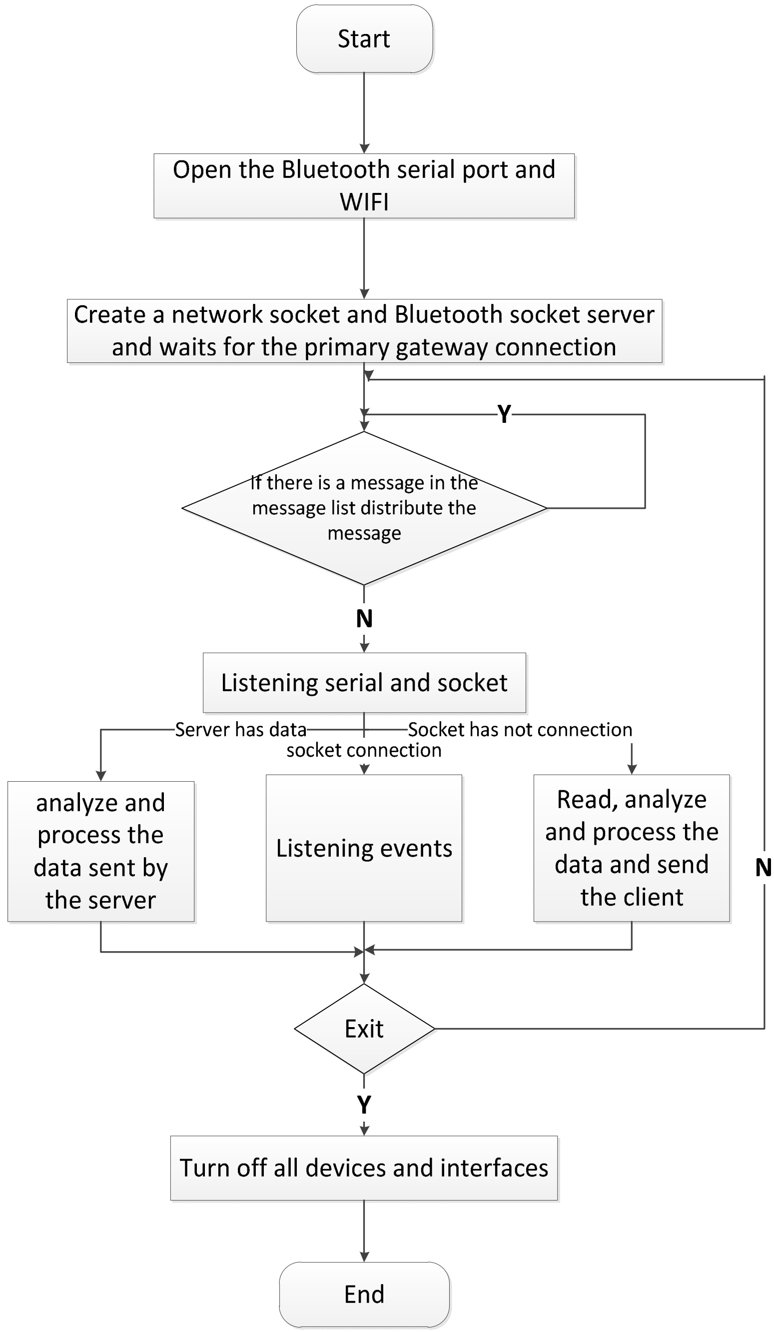

Fig. 8 Bluetooth phone connection

Conclusions

Methods based on visual art quad-rotor aircraft targeting systems in this article is designed for the four-rotary-wing aircrafts, which's a practice of the theory of intelligent automation technology.

The resulting system is the integration of Image Processing Module, Bluetooth Module, Aircraft Control Module. Bluetooth Module send the picture received from the phone to FPGA for further processing. Then the resulting signal of analysis can be used to control the vehicle. But there is no program of Bluetooth driver section in the Bluetooth Communication Module, it's hard for the communication of Bluetooth Module and FPGA. The data sent from mobile phone to control the aircraft is not so accurate , so it's not good to achieve remote control. The lack of these two aspects is the key points that needed to go further researching in the future.

Acknowledgements

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