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Research on Multi-level Inverter of Multi-terminal Switch Network and Extension Topology

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***Abstract*—Due to multilevel inverters can have more levels of output voltage at the output waveform, closer to sine waves, and with small output waveform THD, and low voltage stress, low system advantages of EMI, multilevel inverters are widely recognized, and get a certain application. Based on the analysis of the characteristics of the basic multi-level inverter topology and the scope of application, this paper explores the idea and method of multi-level inverter topology using multi-terminal switch network. By comparing the new topology and basic topology, it can be seen that this new multi-level inverter topology is easy to expand, requiring small filter inductance volume and inductance, loss and low cost, which is an important direction for the development of topological circuits. The new multi-level topology has broadened the research scope of multi-level inverter topology and created new ideas and directions for multi-level topology research, which provides theoretical guidance for further scientific research and engineering applications.**

Keywords-multi-level inverter; power topology; multi-port switch network

I. INTRODUCTION

Main circuit topology is the core of the inverter, inverter modeling, and control algorithms are all around the topology to improve system performance. The traditional two-level inverter topology has long been widely used, but there are shortcomings such as large switching losses, large filter inductance and large output harmonics. Multi-level inverter output has more levels of output level, small output waveform THD, low system EMI, higher power density and waveform closer to the sine wave and other advantages, so it is favored by the researchers. Firstly, the characteristics of three basic 3-level inverter topologies are analyzed and summarized. Then, the multi-terminal switch network is applied to traditional three-level and two-level inverter topology, and proposed a new multi-level topology family. The topological mode of type II 5-level inverter using multi-terminal switch network is analyzed emphatically, and the result of theoretical analysis is verified by simulation. It is very important to further improve the performance of multi-level inverter by further studying the topology of multi-level inverter using multi-level inverter topology.

II. BASIC 3-LEVEL INVERTER TOPOLOGY

A. Diode-Clamped Topology

Diode-clamped 3-level inverter topology is the earliest development and the most widely used multi-level inverter topology. This topology consists of multiple power devices in series, according to certain switch logic to produce the number of output voltage level. For an n-level diode-clamped inverter, the DC side requires (n-1) partial voltage capacitors, 2(n-1) switching devices per device, 2(n-1) antiparallel diodes and (n-1) * (n-2) clamp diodes.

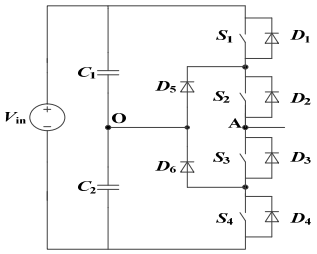


FIGURE. I. DIODE- CLAMPED 3-LEVEL TOPOLOGY

In the industry, it usually uses the following three methods: sinusoidal-triangular carrier modulation [2-4], space vector modulation combined with three-dimensional algorithm [5-7], the specific harmonic elimination method [8-10].It has the following characteristics: power switching devices bear the voltage stress is small; It requires a large number of clamp diodes while clamping the use of diodes to increase the total loss, reducing the conversion efficiency; There is a problem of DC capacitor voltage imbalance; It is difficult to ensure of the capacitor pressure the DC side; Its circuit structure is simple; It is more used in the UPS and photovoltaic inverter; It is mainly 3-level circuit, generally not more than five levels.

B. Flying-Capacitor-Clamped Topology

Flying-capacitor-clamped topology uses the capacitor instead of the diode on the switch tube voltage clamp.

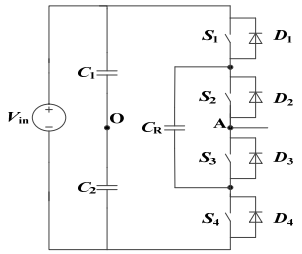


FIGURE II. FLYING-CAPACITOR-CLAMPED 3-LEVEL TOPOLOGY

There is no diode clamp type circuit inside and outside the power tube turn-off voltage imbalance and clamp diode reverse recovery problem. For an n-level flying-capacitor-clamped inverter, it only requires a DC voltage source, the DC side requires n-1 voltage divider, 2(n-1) switching devices per phase, 2(n-1) anti-parallel diodes and (n-1)*(n-2)/2 clamp capacitors. 3-level flying-capacitor-clamped topological phase shift is often used with PWM modulation [11].

Flying-capacitor-clamped inverter has the following characteristics [12]: It improves the equivalent switching frequency, switching loss is small, high efficiency; It has a large number of switch state combinations of redundancy that can be used for voltage balance control; It requires a large number of capacitors, so the circuit is bulky; It has the problem of capacitance voltage balance; It is actually applied less, and it can be used for high voltage DC transmission and frequency control.

C. Cascaded H-bridge Topology

Multi-level cascaded H-bridge inverter is also known as chain inverter. It is a common single-phase full-bridge (H-bridge) inverter as the basic unit, which the DC power each basic of unit is independent of each other. It consists of a number of power units directly connected in series, the more the number of series, the output level is also more. For an n-level cascaded H-bridge multilevel inverter, 2 (n-1) switching devices and 2 (n-1) anti-parallel diodes are required per phase.

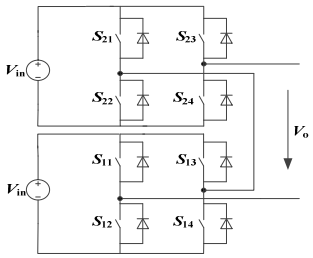


FIGURE III. CASCADED H-BRIDGE3-LEVEL TOPOLOGY

The cascaded H-bridge 3-level inverter topology consists of multiple 2-level H-bridge power units cascaded [13]. According to the switch state of the different combinations, each H bridge can output three levels -Vin, 0 and Vin..Two H-bridge series can be output a total of five levels:-2Vin, -Vin, 0, +Vin, +2Vin.Because this topology has the modular intrinsic characteristics, the modulation method mainly uses the phase shift PWM (PS-PWM) [14]. It can also be used with hybrid modulation technology, an H-bridge unit operating at the frequency, the other working at high frequencies, which can further improve the topology of the conversion efficiency [15-16]. Cascaded H-bridge requires fewer devices, it does not have the problem of no midpoint voltage balance, its control strategy is simple; it requires independent power supply, It is suitable for 7-level and above, it is the most widely used in the photovoltaic industry.

III. A MULTI-LEVEL INVERTER WITH MULTI-TERMINAL SWITCH NETWORK

A. Construction of Multi-Terminal Switch Networks

According to the previous analysis, the traditional multi-level inverter is a prominent problem is that with the increase in the number of levels, it needs the number of devices increases. The large number of switching devices increases the size and cost of the system, and the modulation circuit becomes extremely complex. Therefore, the core problem of multilevel inverter topology research is how to reduce the number of devices used in the same output level, or get more output levels under the same number of devices. In the multi-level inverter topology research, domestic and foreign scholars continue to try to introduce some new technology and try to use less power switch to produce higher quality output waveform, which is one of the research focus of multi-level inverter [17]. Researchers have introduced the staggered parallel technique and coupling inductance in the switching power supply into the single-phase half-bridge inverter topology. At the same time, the concept of the multi-terminal switch network is proposed by combining the construction of the power device and the magnetic coupling. Single-phase half-bridge inverter using a 3-terminal switch-network (3TSN) is shown in Figure 4. Its basic unit consists of four power switch tubes and their body diodes, two input filter capacitors, an inverting coupled two-winding transformer and an output filter inductor.

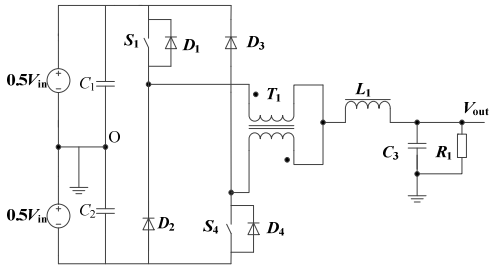


FIGURE IV. SINGLE-PHASE HALF-BRIDGE INVERTER TOPOLOGY USING 3TSN

If this switch network is applied to traditional 3-level and 2-level inverter topology, more new multi-level topologies can be proposed.

B. Diode-Clamped 5-level Inverter Using 3TSN

Based on the basic Diode-Clamped topology, if you add 3TSN, you can form a new diode-clamped 5-level inverter topology as shown in Fig.5. This topology consists of four power switches S1, S2, S3, S4 and their body diodes D1, D2, D3, D4, four power diodes D5, D6, D7, D8, two input filter capacitors C1, C2, an inverting coupled two-winding transformer T1, an output filter inductor L1 and a filter

capacitor C1. Since the inverter topology has two arms, transformers and inductors, the shape is like two letters "I", which is called "II type five level inverter".

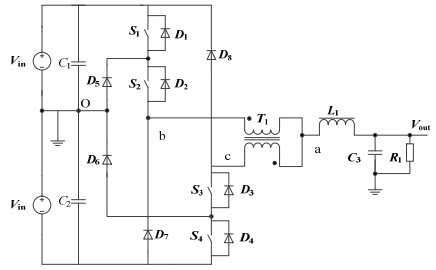


FIGURE V. SINGLE-PHASE II-TYPE 5-TEVEL INVERTER

There are two different operation ranges in the positive half cycle of line frequency. The operation scenarios are described as follows in the condition of: A) duty cycle of S1 D < 0.5, and B) D > 0.5.

1) Duty Cycle of S1 (D) < 0.5

In this operation range, the single-phase II-type 5-level inverter has four switching modes in a complete switching period, as shown in Fig.6., where S1, S2, S3 and S4 are drive signals of 4 active power switches, Vao is the inverter middle-point voltage, Vbc is the winding voltage between two terminals, I_m is magnetizing current, And both of two input voltages are Vin/2, while the output voltage is Vout.

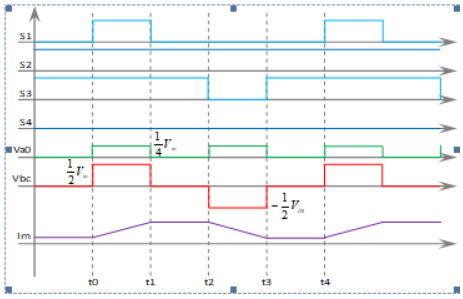


FIGURE VI. POSITIVE HALF OF SINE WAVE PERIOD, D<0.5

a) t0~t1: The power switches S1, S2 and S3 are switched on. As point “b” are connected to the positive pole of input voltage V_{in}, the "c" point potential is the midpoint of the DC bus, so the voltage across the inverting coupling transformer T_1 is $V_{bc} = V_{in}/2$.As a result, I_m is increased with the rate of $(V_{in} * t)/L_m$ linearly. As the inverter middle-point voltage is $V_{ao} = +V_{in}/4$.

b) t1~t2: The power switches S1 with S2 are continuously on. While the power diodes D7 and D8 also continued flow conduction. As both of the point “b” and the point “c” are connected to the middle of the DC bus, the voltage between two terminal of the transformer T_1 is V_{bc} =0, I_m remains no change. The inverter middle-point voltage is V_{ao} =0.

c) t2~t3: The power switches S2 is continuously on, while the power diodes D6 and D7 also continued flow conduction. As point “b” is the midpoint of the DC bus, while the point "c" point is connected to the positive pole of input voltage V_{in}, the voltage between two terminal of the transformer T_1 is $V_{bc} = -V_{in}/2$, I_m is decreased with the rate of$(V_{in} * t)/L_m$ linearly. The inverter middle-point voltage is V_{ao} =+V_{in}/4.

d) t3~t4: The power switches S1 with S2 are continuously on while the power diodes D7 and D8 also continued flow conduction. As both of the point “b” and the point “c” are connected to the middle of the DC bus, the voltage between two terminal of the transformer T_1 is V_{bc} =0, I_m remains no change. The inverter middle-point voltage is V_{ao} =0.

From the above analysis, the inverter middle-point voltage V_{ao} is with two levels of 0 and $+V_{in}/4$. The current I_m can flow in both directions, so that the transformer T_1 can achieve a reliable reset. Based on the theory of volt-second balance of inductors, the averaged output voltage can be obtained by the integration calculation.

$$V_{out} = \frac{2}{T}[\int_{t0}^{t1}\frac{1}{4}\cdot V_{in}\cdot dt + \int_{t1}^{t2} 0\cdot dt]$$
$$= \frac{2}{T}\cdot\frac{1}{4}\cdot V_{in}\cdot D\cdot T$$
$$= \frac{V_{in}}{2}\cdot D \quad (1)$$

2) Duty Cycle of S1 (D) > 0.5

In this operation range, the topology has four switching modes in a complete switching period, as shown in Fig. 7.

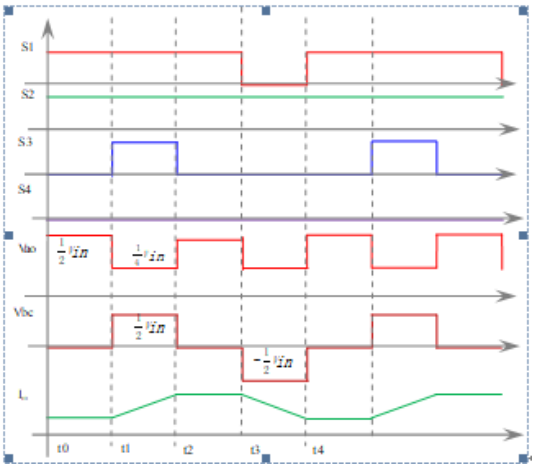


FIGURE VII. POSITIVE HALF OF SINE WAVE PERIOD, D>0.5

a) t0~t1: The power switches S1, S2 are switched on. As both of the point “b” and the point “c” are connected to the positive pole of input voltage V_{in} , so the voltage across the inverting coupling transformer T_1 is V_{bc} =0.As a result, I_m remains no change. As the inverter middle-point voltage is V_{ao} =+V_{in}/2.

b) t1~t2: The power switches S1, S2 and S3 are switched on. As point “b” is connected to the positive pole of input

voltage V_{in} ,while the point "c" is the midpoint of the DC bus, the voltage between two terminal of the transformer T_1 is V_{bc} =+V_{in}/2. I_m is increased with the rate of (V_{in} * t)/L_m linearly. The inverter middle-point voltage is V_{ao} =+V_{in}/4.

c) t2~t3: The power switches S1 with S2 are continuously on, while the power diodes D6 continued flow conduction. As both of the point “b” and the point “c” are connected to the positive pole of input voltage V_{in} , the voltage between two terminal of the transformer T_1 is V_{bc} =0, I_m remains no change. The inverter middle-point voltage is V_{ao} =+V_{in}/2.

d) t3~t4: The power switch S1 is continuously on, while the power diodes D6 and D7 also continued flow conduction. As point “b” is the midpoint of the DC bus ,while the point "c" is connected to the positive pole of input voltage V_{in}, the voltage between two terminal of the transformer T_1 is V_{bc} =-V_{in}/2, I_m decreased with the rate of (V_{in} * t)/L_m .The inverter middle-point voltage is V_{ao} =+V_{in}/4.

From the above analysis, the inverter middle-point voltage Vao is with two levels of +Vin/4 and +Vin/2, .The current Im can flow in both directions, so that the transformer T1 can achieve a reliable reset. Based on the theory of volt-second balance of inductors, the averaged output voltage can be obtained by the integration calculation.

$$V_{out} = \frac{2}{T}[\int_{t0}^{t1}\frac{1}{2}\cdot V_{in}\cdot dt + \int_{t1}^{t2}\frac{1}{4}\cdot V_{in}\cdot dt]$$
$$= \frac{2}{T}\cdot[\frac{1}{2}\cdot V_{in}\cdot(D-\frac{1}{2})\cdot T + \frac{1}{4}\cdot V_{in}\cdot(1-D)]$$
$$= \frac{V_{in}}{2}\cdot D \qquad (2)$$

From the equations (1) and (2), the calculated results of the inverter middle-point voltage Va0 at the conditions of D<0.5 and D>0.5 in the positive half grid period of sine wave output are total same. And The inverter middle-point voltage is with three levels of 0, +Vin/4 and +Vin/2.

TABLE I. SWITCHING COMBINATIONS

Condition	Switching Combinations						
	Operation mode	***S1***	***S2***	***S3***	***S4***	***Vbc***	***Vao***
D<0.5	1	1	1	1	0	*+Vin*/2	*+Vin*/4
	2	0	1	1	0	0	0
	3	0	1	0	0	*-Vin*/2	*+Vin*/4
	4	0	1	1	0	0	0
D>0.5	1	1	1	0	0	0	*+Vin*/2
	2	1	1	1	0	*+Vin*/2	*+Vin*/4
	3	1	1	0	0	0	*+Vin*/2
	4	0	1	0	0	*-Vin*/2	*+Vin*/4

By exchanging the duty cycle of S1 to S4, the operation modes in the negative half grid period of sine wave output are similar to the positive counterpart. In the negative half grid line cycle, the inverter middle-point voltage is with three voltage levels of 0,-Vin/4 and -Vin/2. Hence Vao can be obtained with five levels of+Vin/4,+Vin/4,0,-Vin/4 and -Vin/2.in the full grid line period of sine wave output.

With only 4 active power switches, 5-level operation can be obtained in the proposed topology.

C. Simulation Analysis

The conventional SPWM modulation scheme can be applied in the single-phase II-type 5-level inverter using 3TSN. The simulated circuit of single-phase II-type 5-level inverter using 3TSN is shown in Fig.8. The key simulated waveforms of single-phase II-type 5-level inverter using 3TSN are shown in Fig.10 to validate the theoretical analysis.

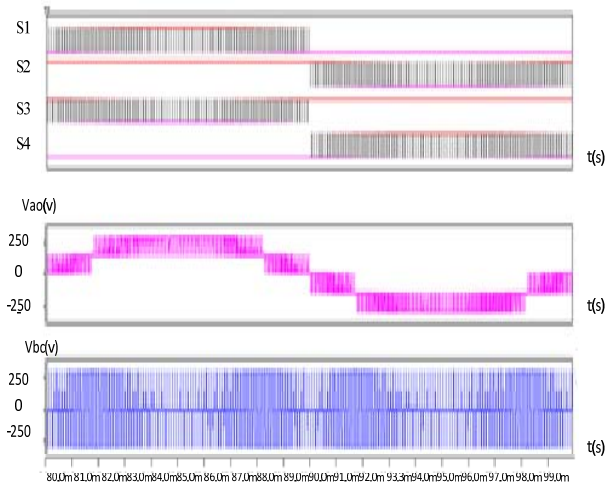
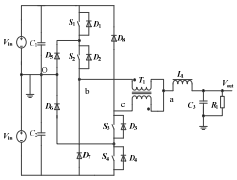
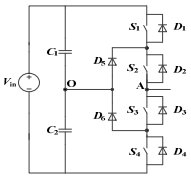


FIGURE VIII. KEY SIMULATION WAVEFORMS OF SINGLE-PHASE II-TYPE 5-LEVEL INVERTER

Meanwhile, the inverter middle-point voltage exhibits five voltage levels, which are 0, +Vin/4, +Vin/2. in the positive half grid cycle, and 0, -Vin/4 , -Vin/2 in the negative half cycle. Therefore, the volume of output inductor is much small and the output harmonics can be reduced.

By comparing the new topology and basic topology, If a new multi-level inverter topology consisting of two diodes and an inverting coupled two-winding transformer T1 is added to the original basic three-level topology circuit, it can obtain 5-level output.

TABLE II. PERFORMANCE COMPARISON

Topology	**Performance Comparison**	
	II-type 5-level	***I-type 3-level***
Circuit		
Number of levels	5	3
Number of switches	4	4
Number of diodes	4	2
Power supply requirement	±Vin/2	±Vin/2
Switch voltage stress	Vin	Vin

D. New Multi-Level Inverter Topology Family Using Switch Networks

1) Novel capacitor clamped multilevel topology using 3tsn

If a new three-terminal switch network is added to the capacitor-clamped multi-level topology, a new capacitive clamped multi-level topology is formed, as shown in Figure 9. This type of topology consists of four power switches S1, S2, S3, S4 and its body diodes D1, D2, D3, D4, four power diodes D5, D6, D7, D8, two flying capacitors C3, two input filter capacitors C1, C2, an inverting coupled two-winding transformer T1, an output filter inductor L1 and a filter capacitor C5.

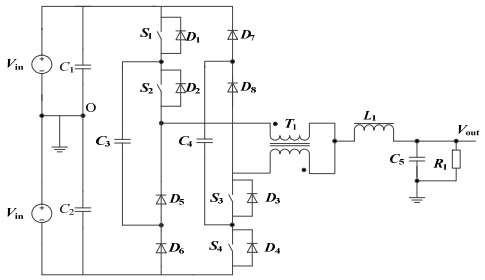


FIGURE IX. SINGLE-PHASE FLYING CAPACITOR 5-LEVEL INVERTER

2) A cascaded five - level topology using 3TSN

If a 3TSN is used in a basic cascade three-level topology, a new cascaded 5-level topology is formed, as shown in Figure 10. This topology consists of four power switches S1, S2, S3, S4 and their body diodes D1, D2, D3, D4, four power diodes D5, D6, D7, D8, four input filter capacitors C1, C2, C3, C4, two inverting coupled two-winding transformers T1, T2, two output filter inductors L1, L2 and a filter capacitor C5.

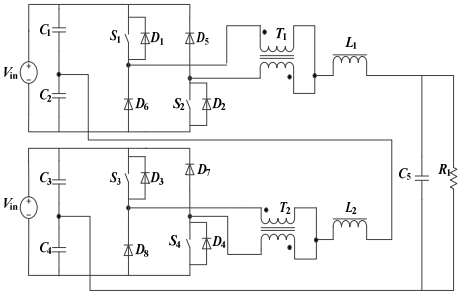


FIGURE X. SINGLE-PHASE CASCADED H-BRIDGE 5-LEVEL INVERTER

IV. CONCLUSION

Multi-terminal switching network multilevel inverter topology does not use the traditional method of increasing power devices to increase the number of levels. It combines power devices with a magnetic coupling to build a way that eliminates the need for clamping diodes and clamp capacitors. It uses less power switching devices to achieve as many output levels as possible. The topology is simple and easy to expand, with high power density and low cost. Using a simple and reliable SPWM modulation strategy and conventional filtering, it can obtain sine wave output voltage. It improves the output filtering inductor ripple frequency by using appropriate phase shift control and improves and improves the traditional topology output voltage level. The topology has the advantages and characteristics of multi-level topology, which reduces the output filter inductance volume and inductance,

reduces its power consumption and cost, and can improve the output harmonics and improve the inverter efficiency. The introduction of multi-terminal switch network has created a new idea and direction for the research of multi-level topology, broadened the research scope of multi-level inverter topology, and pointed out a new research direction to improve the performance of multi-level inverter.

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