Design of the Digital Baseband of RFID Reader Based on FPGA

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Abstract. In this paper, the digital baseband system of RFID reader is researched and designed, and finally realized with FPGA according to the ISO15693 protocol. The data encoding and decoding modes and checking methods in the protocol are analyzed. The top-down design method is used to design the reader's digital baseband system, including the PPM encoding and CRC checking in the sending module, and the Manchester decoding in the receiving module. On this basis, the system is verified by FPGA. As the price of the RF tag is reduced, the reader's digital baseband system will be applied to the commodity tracking system.

Introduction

Radio frequency identification technology (RFID) is one of the key technologies to realize the Internet of things. It achieves the goal of target recognition through radio frequency signal. Unlike traditional barcode recognition technology, magnetic card recognition technology and IC card recognition technology, RFID is a wireless identification technology. It has many advantages, such as non-contact, anti-interference ability, and can recognize multiple objects at the same time. It is one of the most important automatic recognition technologies at present. It has been widely used in all walks of life, such as transportation, anti-counterfeiting and logistics. In the RFID system, the tag receives the radio frequency signal sent by the reader and sends the information stored in the tag by the energy obtained by the induced current. The reader reads the information and decodes it, and sends the information to the computer for data processing [1].

FPGA has great flexibility, repeatable programming, high efficiency and low cost. It has become the most widely used ASIC [2]. The existing RFID reader is generally implemented by DSP or ARM architecture, which is complex and is not easy to upgrade. Based on the detailed analysis of the ISO 15693 protocol, the top-down design method is used to give the overall structure of the RFID reader system, especially the design and FPGA implementation of the digital baseband module. The purpose is to apply this digital baseband system to the supermarket commodity anti-theft tracking system.

Analysis of ISO15693 Protocol

Reader to Tag. In the protocol, the data encoding of reader to tags shall be using pulse position modulation [3]. The value of one single byte shall be represented by the position of on pause. The position of the pause on 1 of 256 successive time periods of 256/13.56MHz (18.88us), determines the value of the byte. In this case the transmission of one byte takes about 4.833ms. Fig. 1 illustrates this pulse position modulation technique. In Fig. 1 data=8`hE1=8`b11100001=225 is sent by the reader to tag.

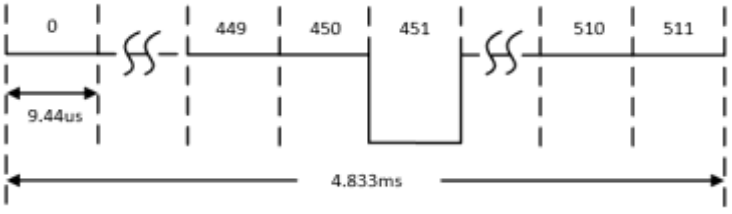

Figure 1. 1 of 256 coding mode

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Tag to Reader. In the protocol, the data encoding of tag to reader shall be encoded using Manchester coding, according to the following schemes [3]. A logic 0 starts with 8 pulses of 13.56MHz /32 (423.75 kHz) followed by an un-modulated time of 256/13.56MHz (18.88us), see Fig. 2. A logic 1 starts with an un-modulated time of 256/13.56MHz (18.88us) followed by 8 pulses of 13.56MHz /32 (423.75 kHz), see Fig. 3.

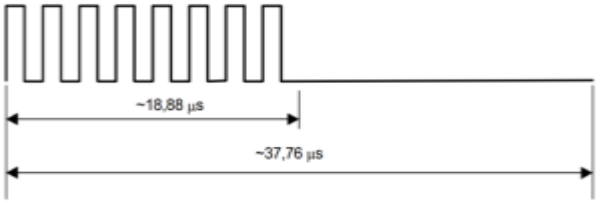

Figure 2. Logic 0

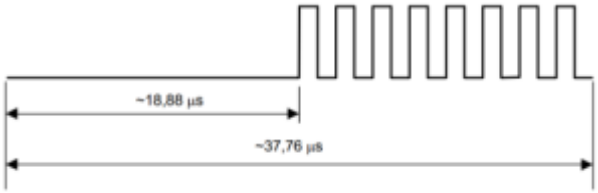

Figure 3. Logic 1

Data Validation. In the process of transferring commands from the reader to the tag, there are often unpredictable data errors caused by external interference. Therefore, the ISO15693 protocol uses cyclic redundancy check (CRC) for error control [4]. The protocol uses CRC-CCITT and the generator polynomial is Eq. 1.

$$g(x)=x^{16}+x^{12}+x^{5}+1 \quad (1)$$

The Design of the Digital Baseband

Based on the actual situation and design requirements, a top-down design method is proposed in this paper. A modular design scheme is proposed to analyze the structure of reader digital baseband circuit. Each module is designed as a unit. Overall, reader's digital baseband system is divided into three parts, including sending module, receiving module and control module. Fig. 4 shows the overall structure of reader's digital baseband. The sending module consists of CRC, PPM encoder and modulator. Receiving module is composed of the demodulator, Manchester decoder, anti-collision and CRC [5].

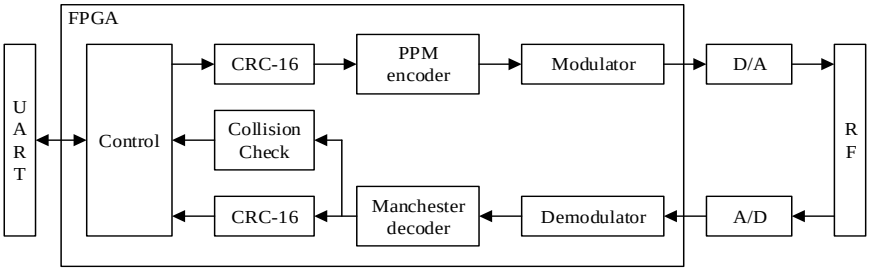

Figure 4. General block diagram of digital baseband system

In the sending module, the controller controls the sending of commands and sends commands to the CRC checking module to generate the checking codes. The checking codes are appended to the command data and then sent to the PPM encoding module for encoding. The completed encoded data is sent to the modulator for ASK modulation. In the receiving module, the demodulator completes demodulation of the data, then sends it to Manchester decoder for decoding. On the one hand, the decoded data is sent to CRC checking module to check the validity of the data. On the other hand, the decoded data is sent into the collision module to make the appropriate collision processing, and send the results into the controller [6]. This design focuses on PPM encoding module, Manchester decoding module and CRC module.

PPM Encoder. Through the analysis of the protocol above, it can be seen that the PPM coding is actually a process of low pulse output by timing. According to the standard time interval defined by the protocol, the timing process can be converted into a counting process. When the clock signal

arrived, the counter began counting and counting to the time to output a low pulse to complete the PPM encoding process.

As shown in Fig. 5, the clock signal is sent into the slot divider to generate the slot signal which is input into the frame divider. The frame divider generates the frame signal according to the preset data, and counts the slot signal. The obtained count value and the preset data are compared by a numerical comparator, and a low pulse signal is output when the two are equal. The pulse signal is passed through a pulse former to obtain the PPM pulse signal, which passes through the pulse shaping filter with slot signal and frame signal to get the encoded PPM signal [7].

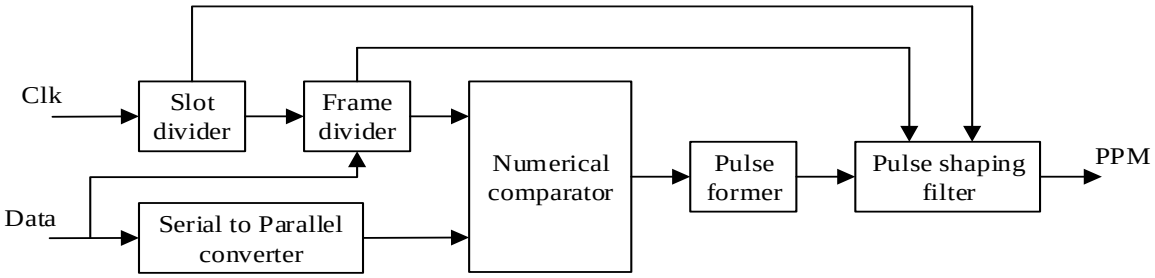

Figure 5. Block diagram of PPM encoding module

Manchester Decoder. Through the analysis of the protocol above, we can see that the data from tag to reader is encoded by Manchester code. In this section, we design the Manchester decoding module in the system according to the Manchester encoding rule. The Manchester code rules the message "0" when the electrical level is changed from high to low, and the information "1" when the level is changed from low to high [8]. As shown in Fig. 6, the reader has to detect the start of the frame (SOF) after receiving the label signal and then start decoding. When the end of the frame (EOF) is detected, the decoding is stopped. Since there is a level jump in the central of each symbol interval, the decoding module requires a sampling clock that is doubled to the data rate. When decoding, a data register is set to store the signals collected by the previous clock and the current clock. When the content of the register is “10”, the output is “0”. And when the content of the register is “01”, the output is “1”.

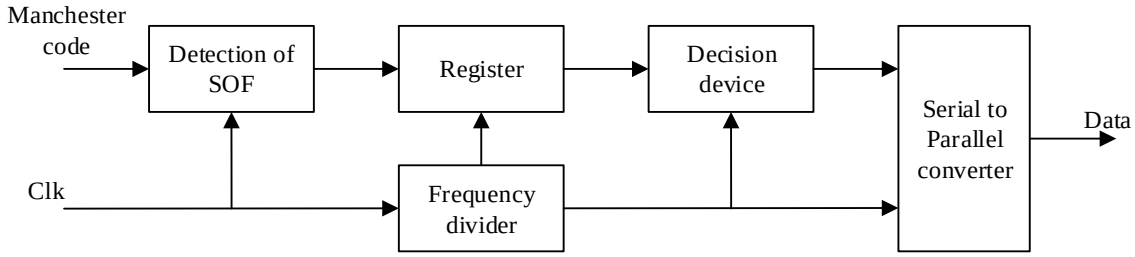

Figure 6. Block diagram of Manchester decoding module

CRC Module. In the process of data transmission between reader and tags, the data could be affected by external interference, resulting in some unpredictable errors. Therefore, ISO15693 protocol using Cyclic Redundancy Check (CRC) to control errors, and the generating polynomial is Eq. 1. CRC module receives k-bit data from reader or tags, generates 16-bit check code according to the generating polynomial. The 16-bit check code will be attached to the end of the original data, constitute (k + 16) bits data. CRC module is shown in Fig. 7, consists of 16-bit register and 3 XOR gates, and the XOR gate is set where the coefficient of generating polynomial is 1 [9]. To generate CRC code, the initial value of the 16-bit register is set 16`hFFFF, then input the k-bit data from low to high in serial mode, the value of 16-bit register is the 16-bit check code required at the end of data input. To CRC calibration, the initial value of 16-bit register is also set 16`hFFFF, then attach the 16-bit check code to the end of the original k-bit data as the (k+16) bits new data, input the new data from low to high in serial mode. If the value of 16-bit register is 16`hF0B8 at the end of data input, shows there is no error in the data transmission, otherwise there are some errors.

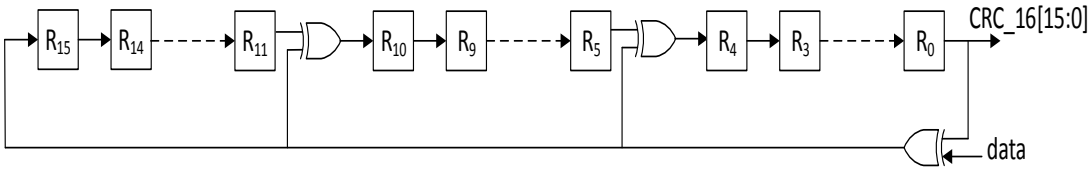

Figure 7. CRC module

The Implementation of Digital Baseband

After the completion of the system design, we need to simulate and verify the circuit, and download the bit stream file to the FPGA chip for debugging [10]. The development environment of this design is Quartus II of Altera. According to the design of the digital baseband system above, we use Modelsim to carry out Verilog coding of each functional module and perform corresponding function simulation.

PPM Encoder. The PPM encoding module is designed and simulated. The data to be coded is 8`hE1= 8`b11100001=225. The simulation result is shown in Fig. 8, and the result is that a low pulse is generated at the 225th of 256 slots, and the simulation result is accurate.

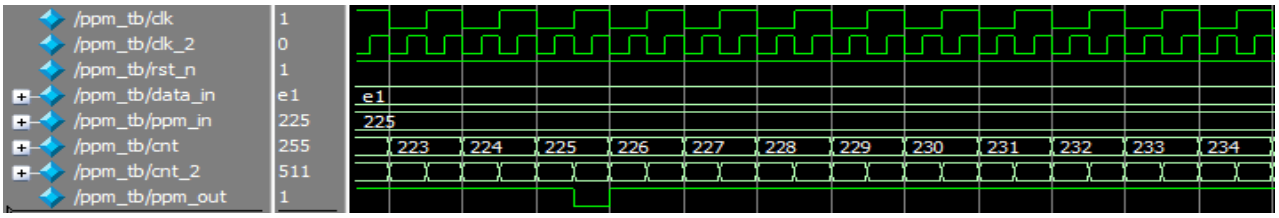

Figure 8. Waveform of PPM encoding

Manchester Decoder. The Manchester decoding module is designed and simulated. The simulation results are shown in Fig. 9. When sof = 1, decoding starts. The input information sequence is data_in = 16`b0101011010101001, the simulation results show that the Manchester decoding output is deman_out = 8`b11100001, and the simulation results are accurate.

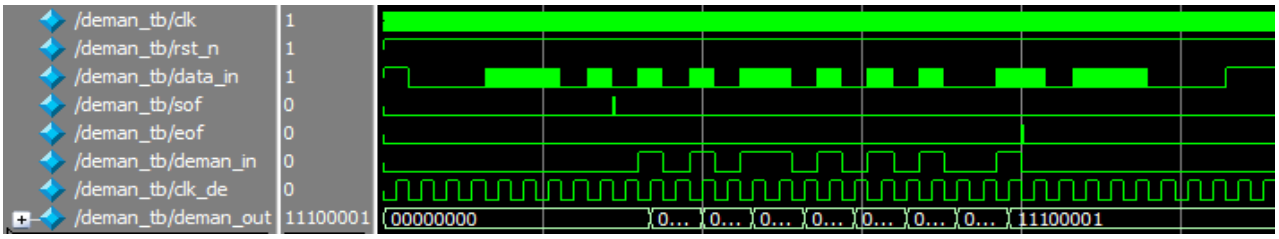

Figure 9. Waveform of Manchester decoding

CRC Module. The CRC module is designed and simulated, and the simulation results are shown in Fig. 10. The input data is data_in= 88`h22200123456789AB04E00B. The data is moved into the register in turn, and the final value of the register is crc_16=16`hBAE3. It is clear that the simulation results are accurate by calculation.

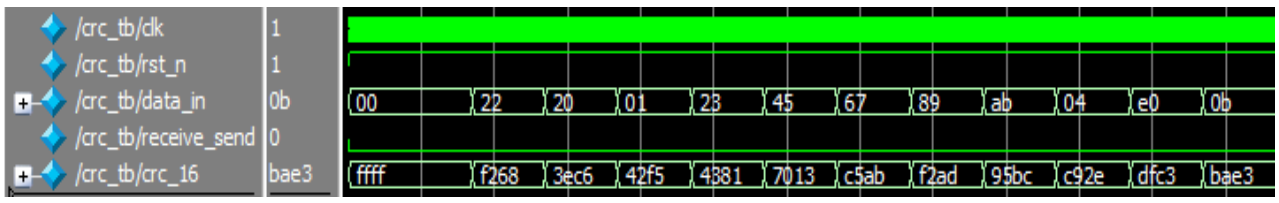

Figure 10. Waveform of CRC

Summary

In this paper, the design of the digital baseband system of the RFID reader is completed by using the top-down design method. Based on the research of the protocol, the encoding, decoding and checking module of the digital baseband system, the specific implementation methods and corresponding simulation results of each module are given. The reader based on the digital baseband system has been applied in practice and has a good effect.

References

[1] Yulan Huang: *RFID Core Technology Based on Internet of Things* (Posts & Telecom Press, China, 2016)
[2] Song Pan, Long Chen, Jiye Hang: *EDA Technology and Verilog HDL* (Tsinghua University Press, China, 2013)
[3] IOS/IEC: *Identification cards - Contactless integrated circuit(s) cards - Vicinity cards - Part 2: Air interface and initialization*, 15693-2. (2010)
[4] IOS/IEC: *Identification cards - Contactless integrated circuit(s) cards - Vicinity cards - Part 3: Anticollision and transmission protocol*, 15693-3. (2010)
[5] Lu Wang: Applied Mechanics and Materials, Vol. 263-266 (2012), p. 2881
[6] Wenfang Zhang: *Design of Baseband and Software of RFID Reader System Compatible with 18000-6C Standard based on FPGA* (MS., University of Electronic Science and Technology of China, China 2015), p.29
[7] Pan He: Modern Electronics Technique, Vol. 33 (2010), p.52
[8] Guofeng Ren: Software Guide, Vol. 12 (2013), p.23
[9] Yan Zhang, Yongfeng Ren, Lei Qi, and Zong Yao: Chinese Journal of Electron Devices, Vol. 38 (2015), p.222
[10] Yuwen Xia: *Verilog Digital System Design Tutorial* (Beihang University Press, China, 2013)