

Implementation of ASK Modulation Modules Based on VHDL

Caihong Liu^{a,*}, Shuangliang Tian^b, Xiuping Chen^c

Northwest Minzu University, Lanzhou, Gansu, China

^acindylu888@qq.com, ^b156610123@qq.com, ^c30788336@qq.com

*Corresponding author

Keywords: Modulation, ASK, Signal, VHDL

Abstract: As a simple, efficient, convenient, easy to implement feature, ASK has its own unique position in the current communication field. The research and application of ASK based communication system is also a hot topic in many research projects. The principle and design method of the study of ASK modulation system is researched in this paper. This paper presents the design and simulation of a modulation module for ASK using VHDL. We used ASK modulation in order to achieve a high transmission speed. The design was simulated using the System Generator for FPGA. The use of simulation can greatly reduce the cost of the experiment.

1. Introduction

In electronics and telecommunications, modulation is the process of varying one or more properties of a periodic waveform, called the carrier signal, with a modulating signal that typically contains information to be transmitted. In general telecommunications, modulation is a process of conveying message signal, for example, a digital bit stream or an analog audio signal, inside another signal that can be physically transmitted. Modulation of a sine waveform transforms a narrow frequency range baseband message signal into a moderate to high frequency range passband signal, one that can pass through a filter.

In digital modulation, an analog carrier signal is modulated by a discrete signal. Digital modulation methods can be considered as digital-to-analog conversion and the corresponding demodulation or detection as analog-to-digital conversion. The changes in the carrier signal are chosen from a finite number of M alternative symbols.

2. Features of VHDL

VHDL (VHSIC Hardware Description Language) is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits. VHDL can also be used as a general purpose parallel programming language.

VHDL is commonly used to write text models that describe a logic circuit. Such a model is processed by a synthesis program, only if it is part of the logic design. A simulation program is used to test the logic design using simulation models to represent the logic circuits that interface to the design. This collection of simulation models is commonly called a testbench.

The key advantage of VHDL, when used for systems design, is that it allows the behavior of the required system to be described and simulated before synthesis tools translate the design into real hardware. Another benefit is that VHDL allows the description of a concurrent system. VHDL is a dataflow language, unlike procedural computing languages such as BASIC, C, and assembly code, which all run sequentially, one instruction at a time. A VHDL project is multipurpose. Being created once, a calculation block can be used in many other projects. However, many formational and functional block parameters can be tuned.

3. Principle of ASK

Amplitude-shift keying (ASK) is a form of amplitude modulation that represents digital data as variations in the amplitude of a carrier wave. In an ASK system, the binary symbol 1 is represented by transmitting a fixed-amplitude carrier wave and fixed frequency for a bit duration of T seconds. If the signal value is 1 then the carrier signal will be transmitted; otherwise, a signal value of 0 will be transmitted.

Any digital modulation scheme uses a finite number of distinct signals to represent digital data. ASK uses a finite number of amplitudes, each assigned a unique pattern of binary digits. Usually, each amplitude encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular amplitude. The demodulator, which is designed specifically for the symbol-set used by the modulator, determines the amplitude of the received signal and maps it back to the symbol it represents, thus recovering the original data. Frequency and phase of the carrier are kept constant.

The symbol can be represented as:

$$s(t) = A(t) \cos(\omega_0 t + \theta) \quad 0 < t \leq T$$

Angular frequency of carrier signal is $\omega_0 = 2\pi f_0$; $A(t)$ is Real time amplitude with the transformation of Baseband modulation signal.

$$A(t) = \begin{cases} A & \text{sending is "1"} \\ 0 & \text{sending is "0"} \end{cases}$$

In digital signal processing, the waveform is rectangular pulse.

As already indicated, the sharp discontinuities in the ASK waveform of Figure 1 imply a wide bandwidth. A significant reduction can be accepted before errors at the receiver increase unacceptably. This can be brought about by bandlimiting (pulse shaping) the message before modulation, or bandlimiting the ASK signal itself after generation. As shown in Figure 1.

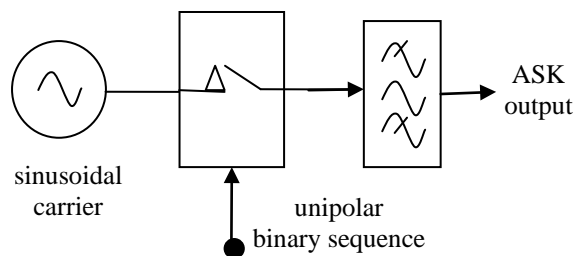


Figure 1 ASK generation method

4. Implementation based on VHDL

4.1 ASK Modulation

A schematic diagram based entry for the desired circuit becomes very difficult to use this method for a large design with hundreds of primitive gates. Hardware description languages provide standard text based expressions of the structure and behavior of digital circuits. Therefore HDL languages are nowadays the preferred way to create FPGA designs. VHDL is a computer programming language designed to illustrate the behavior of field-programmable gate arrays and application-specific integrated circuits of digital systems in electronic design. VHDL describes the performance of electronic components in many areas. VHDL is used to describe precise aspects of electrical circuit behavior in order to create a VHDL simulation model. Incorporated with schematics, block diagrams and system-level VHDL descriptions, the VHDL simulation model can be used as the foundation for building larger circuits.

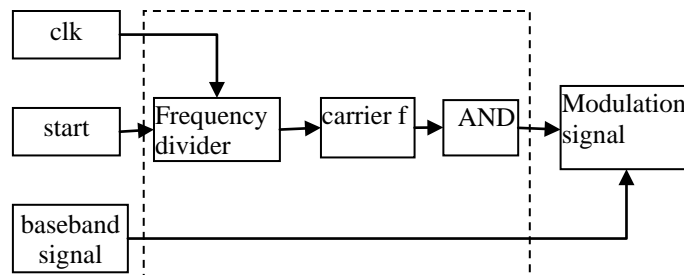


Figure 2 Modulating block diagram

4.2 Program Code

```

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
entity ASK is
port( clk, start, x :in std_logic;
      y :out std_logic);
end ASK;

architecture modulation of ASK is
signal q:integer range 0 to 3;
signal f :std_logic;
begin
process(clk)
begin
if clk'event and clk='1' then
if start='0' then q<=0;
elseif q<=1 then f<='1';q<=q+1;
elseif q=3 then f<='0';q<=0;
else f<='0';q<=q+1;
end if;
end if;
end process;
y<=x and f;
end modulation;

```

5. Conclusion

Before implementing the designed circuit in the FPGA chip on the board, it is prudent to simulate it to ascertain its correctness. Quartus II software includes a simulation tool that can be used to simulate the behavior of a designed circuit. The simulator applies the test vectors to a model of the implemented circuit and determines the expected response. As shown in Fig 3.

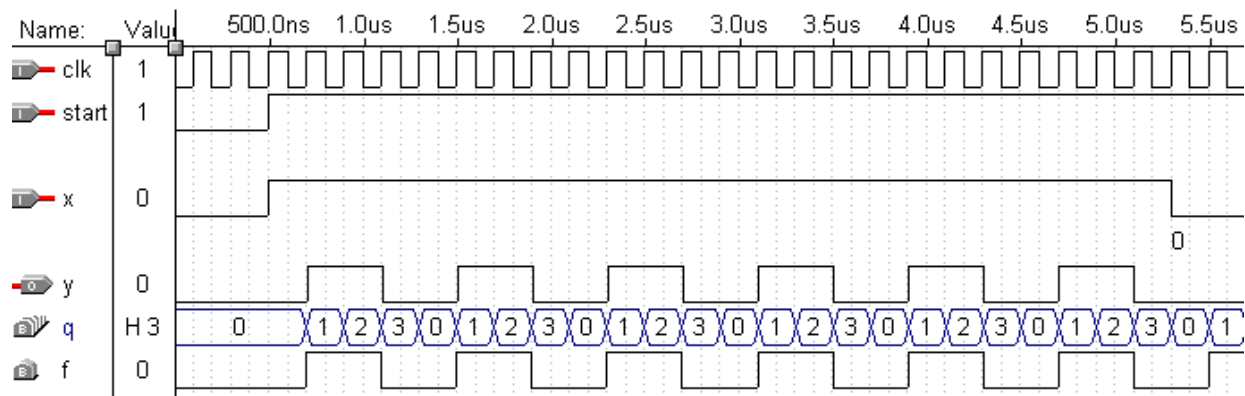


Figure 3. Simulation Results

Compared with traditional methods of ASK modulation, modules based on VHDL has lots of advantages. The simulation results are the same as expected, that is, it is completely feasible to implement the modulation function of ASK on CPLD. The design of the ASK modulation system is stable.

Acknowledgments

This work was supported by “the Fundamental Research Funds for the Central Universities No. 31920170009”. This work was supported by “the Fundamental Research Funds for the Central Universities No.31920140090”.

References

- [1] Deependra Pandey, Kamlesh Kumar Singh, Implementation of DTW algorithm for voice recognition using VHDL, in International Conference on Inventive Systems and Control (ICISC), Coimbatore, India,2017, p. 1 - 4.
- [2] Lester Kalms, Khaled Mohamed, Diana Göhringer, Accelerated Embedded AKAZE Feature Detection Algorithm on FPGA, In: Proceedings of the 8th International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies, Bochum, Germany,2017, p. 123 - 127.
- [3] Hoda A. Alkharizmi, Martin M. Lauridsen (2013) Cryptanalysis of the SIMON Family of Block Ciphers: Presented in PhD summer school titled ‘Theoretical and Practical Topics in resources-efficient Cryptography.
- [4] Mohammad Salehi and Alireza Ejlali, A Hardware Platform for Evaluating Low- Energy Multiprocessor Embedded System Based on COTS Devices, IEEE Transactions on Industrial electronics, Vol. 62, No.2 February 2015.
- [5] Manjusha M. Kinage; D. G. Khairnar, Design and implementation of FPGA soft core processor for low power multicore Embedded system using VHDL, in International Conference on Automatic Control and Dynamic Optimization Techniques (ICACDOT), Pune, India,2017, p. 328 -332.