ATLANTIS PRESS

Advances in Engineering Research, volume 149

2nd International Conference on Mechanical, Electronic, Control and Automation Engineering (MECAE 2018)

Design Method of Computing Acceleration Module Based on Loongson 3A1500

Yanpeng Wang [a], Laixin Zhang [b]

Jiangsu Automation Research Institute, Lianyungang 222061, China.

[a]wyp716@126.com, [b]13912161856@139.com

Keywords: Rugged computers, Loongson 3A1500, FPGA, Computing acceleration, High performance.

Abstract. To improve the computing capacity of domestic rugged computers, the present paper provides a design method of computing acceleration module based on Loongson 3A1500, and introduces the modular design ideas. The domestic Loongson 3A1500 processor and DDR3 memory are used in the hardware side. The present paper designs the 3A1500 + 2FPGA hardware components mode, and introduces the design of the power and reset circuit. On the software side, using the domestic NeoKylin operating system, the present paper designs an acceleration software that matches the module. Finally, a performance test was taken by comparing the present design to the X86 Core L2400 processor. The performance comparison results show that the present design can significantly improve the calculation performance of the domestic Loongson computer and the average calculation speedup reaches 5 or more, which indicates that the design method is effective. The present design has provided a guidance on the high-performance computing application of the domestic reinforcement computer.

1. Introduction

As military information technology becomes more and more in-depth, the traditional methods of data processing based on CPUs have been hard-pressed to meet the high demands of high-speed computing. The demand for computer technology for high-performance data processing has become increasingly stronger. Complying with the generalized, serialized and modularized design ideas, it is the key research direction that the existing general-purpose computer platforms are compatible with the existing standard systems to enhance the processing power of computers.

Internationally, the development of high-speed computing technology has been relatively mature, and continuously released high-speed processors and GPU-assisted calculation methods. The calculation acceleration effect is very good. However, the hardware and software provided by foreign countries have potential risks and may be set as backdoors and vulnerabilities in processors and software systems [1], posing a serious threat to our equipment and data security.

Deeply excavating the potential of China's own technology [2-3], developing autonomous and controllable technologies with high-speed computing power will be the direction we are trying to make[4]. Now proposed a calculation based on domestic Loongson processor acceleration technology, the use of 3A1500 +2 FPGA mode, with our own Neokylin Linux Desktop Operating System., software and hardware to achieve autonomic control to meet the high-speed computing needs.

2. Design Ideas

In order to improve the generality of the computing and processing, considering both FPGA customization and CPU operating system compatibility, the CPU + FPGA mode [5-6] can give full play to Loongson platform strengths, but also make up for lack of high-performance computing is A Design Idea Suitable for Existing Military Requirements. The design name is Computing acceleration module based on Loongson 3A1500, referred to as Computing acceleration module.

3. Hardware Design

Computing acceleration module based on Loongson 3A1500 block diagram is shown in Fig. 1, with the AMD RS780E + SB710 chipset, Loongson 3A1500 processor as the core [7], constitute the main hardware module framework. The computing acceleration module uses high-speed DDR3 memory chips, combined with two high-performance FPGA chips to improve the ability of computing. The present module follows the standard of 6U VPX, and has a strong anti-harsh environmental capability.

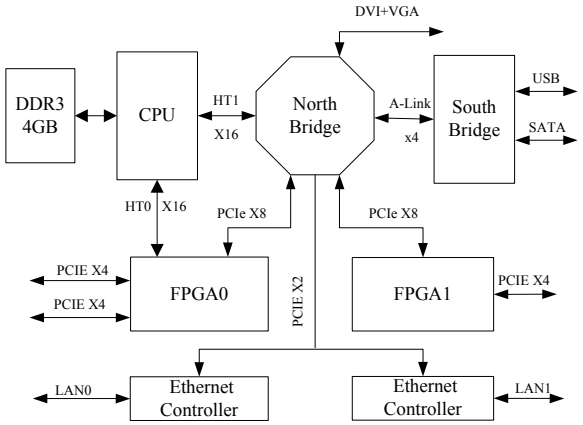

Fig. 1 Hardware block diagram

Loongson 3A1500 processor is 4-core processor, the maximum operating frequency of 1GHz, the chip integrates two 64-bit 400MHz DDR3 controller, two 16-bit HT-800MHz controller. The Loongson 3A1500 dual-HT bus interface provides a high-speed interface for connecting FPGAs to increase computing power. AMD RS780E as the Northbridge, connected with Loongson 3A1500 through Northbridge HT bus interface; Expanded display memory space through DDR3 memory chip; Connected with Intel Ethernet Controller i210 through Northbridge PCIE X1 interface; the Northbridge interconnect to the Southbridge AMD SB710 by A-LINK high-speed bus.

In addition, the Northbridge also provides a PCIE X16 interface (can be split into 2 PCIE X8) and a PCIE X2 interface for the expansion of the system modules and connect to the VPX connector; Northbridge provides display ability, support VGA and DVI display interface. Southbridge integrates a wealth of functional peripheral interfaces, including high-speed A-LINK, USB, SATA and LPC interfaces, USB and SATA directly from the South Bridge output.

In order to achieve a strong computing power computing acceleration module equipped with two FPGA chips, FPGA chips using Xilinx's high-performance VIRTEX-6. FPGA0 communicates with Loongson 3A1500 via HT bus and connects with Northbridge 780E via PCIE X8 bus. Two RapidIO X4 high-speed serial buses are connected to FPGA0 to meet the demand of high-speed data exchange. FPGA1 is connected to the Northbridge 780E via the PCIE X8 bus and goes all the way to the RapidIO X4 high-speed serial bus.

3.1 Power Supply

Power supply as the power and carrier of circuit operation, power supply design is the basis of circuit design. Qualified power supply design, the need to fully understand the various devices and circuits under the premise of the premise, with the power supply voltage, power distribution, ripple and so on. Through the design of the power supply circuit and the conversion power supply, the voltage required for the work of each device, the specific power distribution is shown in Fig. 2.

This module involves more types of power supply, design ideas through a unified power supply, in the module design a variety of power conversion circuits, to provide the required voltage for each device. In this design, according to the characteristics of the VPX architecture, the power input unified by 12V power supply, in theory, to provide more than 300W power, and the module power consumption within 60W, to meet the power requirements.

CPU core voltage CPU_1.1V 12V DC power from the DC-DC module is converted from up to 30A 1.1V power supply. 12V DC-DC module into 1.5V, 2.5V, 1.0V, were given memory, FPGA

power supply. 5V voltage provided by the 12V conversion, after the LDO chip into another board-level voltage.

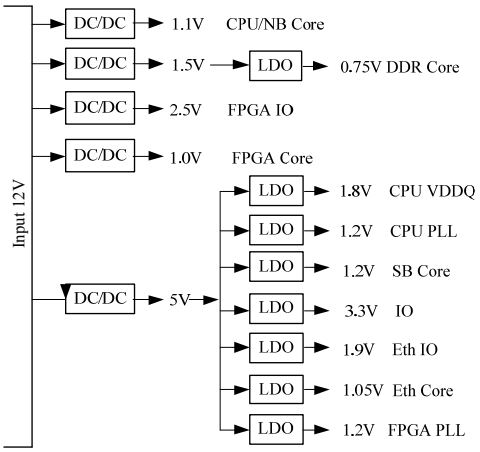

Fig. 2 Power distribution diagram

3.2 Clock Design

The design of the clock device involved in the main Loongson 3A1500, North and South Bridge and FPGA. The Loongson 3A1500 provides the required operating clock through an external crystal oscillator and other clock sources. The external 14.318MHz crystal provides the required operating clock for the southbridge, northbridge, and PCIE devices through an external clock generator. The clock block diagram is given in Fig. 3.

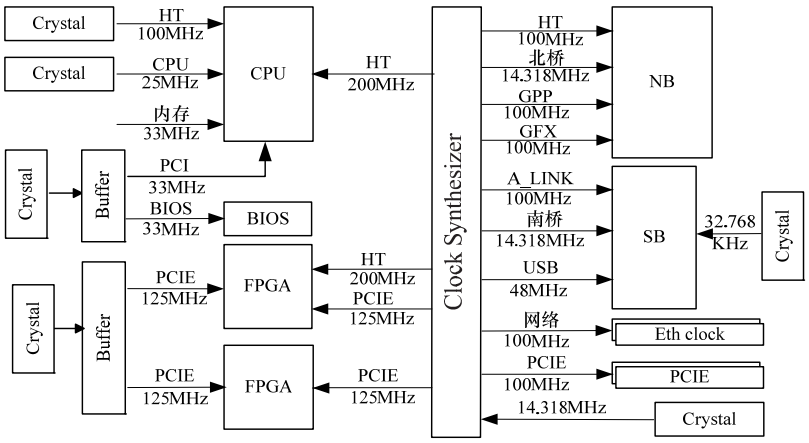

Fig. 3 Clock block diagram

3.3 Reset Design

The paper uses the MAX706 to determine the reset of the entire module. The first power-on reset by the VPX connector to provide power and the original reset signal, the main module MAX706 is responsible for the completion of the CPU, the South Bridge and the reset circuit peripherals, the chip integrates strict timing logic control circuit, you can ensure that the system according to strict Reset the timing, to complete a stable start. The system can control the overall reset of the system through the CPU's GPIO signal. System reset circuit block diagram shown in Fig 4.

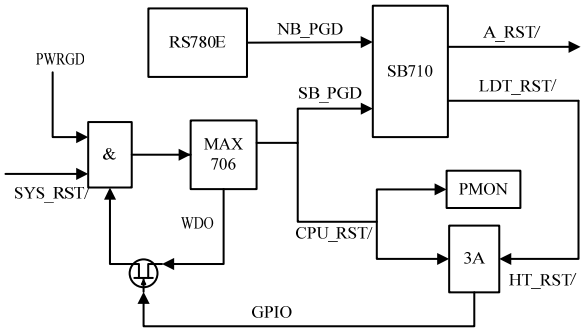

Fig. 4 Reset block diagram

3.4 DDR3 Design

In order to improve the ability of the module to withstand harsh environments, the paper uses a full-board DDR3 chip for dual-channel design. Loongson 3A1500 processor integrated two memory controller MC0 and MC1, memory controller MC can provide a standard DDR3 memory device interface, which can realize the data transmission with the external DDR3 chip.

Loongson 3A1500 supports up to 4 chip select cs, 16-bit ranks of the address bus and 3 for the logical bank bus. This design uses 10 pieces of DDR3 memory particles, single-chip capacity 4Gb, 16-bit data width. Of which 8 composed of 4GB running memory, two ECC error correction memory composition. The design of memory circuits, memory frequency set to 400MHz.

4. Software Design

In order to realize the calculation acceleration method based on Loongson 3A1500 proposed in this paper, the software design of the calculation acceleration module is needed. Calculation of acceleration module software design includes operating system-related design and calculation of accelerated software design. For the operating system, aimed at the localization of software and hardware needs, choose the better developed in recent years successful Neokylin Linux Desktop Operating System , based on the successful Neokylin for Loongson 3A1500 platform operating system migration and driver design; calculation of accelerated software design, Can give full play to computing acceleration module dual FPGA excellent computing performance, coordinate the system to allocate resources, the FPGA into the calculation process.

4.1 Operating System Migration and Driver Design

Neokylin Linux Desktop Operating System is based on a system developed by the Linux kernel, so its driver and software development basically follow the Linux. The kernel transplant technically takes the open source Linux as the mainstay, transplants the development by the way of cross compiler, and modifies the code of processor initialization and hardware driver, and transplanted the Neokylin to the processor architecture. With Loongson 3A1500 processor hardware platform features, design and development of Loongson 3A1500 processor support module. Mainly to complete the processor initialization code, related driver changes to support network functions, support for JFFS2, YAFFS file system [8], modify the design MTD partition, so that the kernel can mount the file system on the storage device.

4.2 Calculation Acceleration Software Design

Computation acceleration module contains CPU and FPGA, CPU executes software instructions, FPGA can be configured as different structure of hardware accelerator. The configuration and operation of the hardware accelerator are controlled by the CPU (software), and put forward higher requirements on the software writing. The overall configuration process and the interface details of the accelerator need to be fully understood before completing the program construction. Hardware and software co-simulation shielding the hardware details, providing a hardware-transparent programming model, reconfigurable hardware in the form of a function of the abstraction, that is, the hardware programming, simple call hardware functions can be reconfigurable hardware. The

hardware functions are used in the same way as the functions in other software libraries. The details of the entire underlying hardware are transparent to them [9].

Hardware functions need to provide the appropriate hardware and software support environment, according to the hierarchical structure shown in Fig. 5 to support the design of hardware transparent reconfigurable system. The entire system is divided into five layers, the following application layer is the basic hardware and software system-on-chip structure is universal. For different applications, we only need to write the appropriate application. The functions of each layer are as follows:

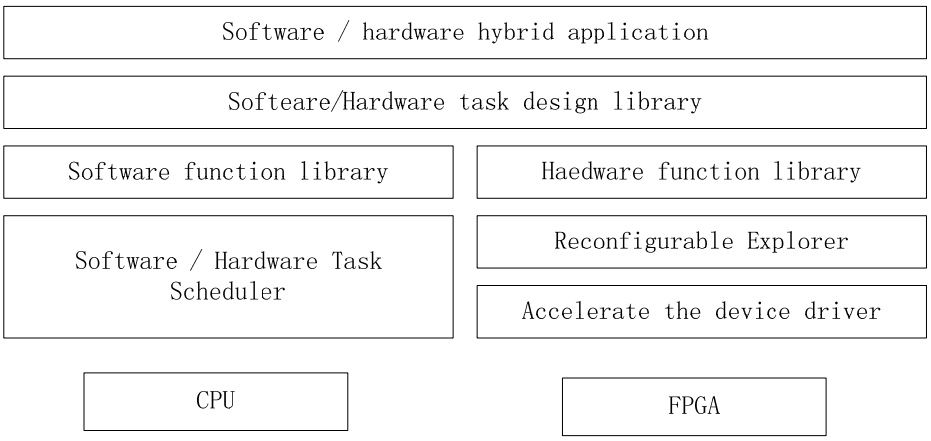

Fig. 5 Calculation of acceleration technology composition

Hardware and software task design library provides a mixed-task programming interface, combined with software libraries and hardware functions library, according to the traditional software programming, design a highly mixed hardware and software systems. The hardware / software task scheduler and reconfigurable resource manager manage hardware function calls, operating states, and so on, and track and manage reconfigurable resources. There are essential differences between the hardware functions and the software functions based on the operation modes and the physical functions. The software functions are a set of instructions for serial execution. The hardware functions are two-dimensional logic circuits and can be executed synchronously with the CPU and added to the corresponding hardware function management module Establish a unified software and hardware operation process. Reconfigurable Resource Manager should keep track of the use of reconfigurable resources, allocating the appropriate resources for the invoked hardware functions.

5. Performance Comparison Test

The innovation of this paper is that on the Loongson 3A1500 platform, the design of the Loongson 3A1500 module is accelerated by dual FPGAs, while the existing software and hardware environment is extended. In this way, the computational performance of domestic-made computers is improved. Therefore, in the calculation of acceleration modules for performance testing, the focus of the module FPGA acceleration test.

The calculation of acceleration module approach in this paper is the two FPGAs continue to perform FFT [10], DES encryption, RK differential equations, Solutionπ, Quick sore and other algorithms, test and calculate the time consumption of the time-consuming For comparison, the calculated acceleration ratio data.

Speedup τ = time before acceleration / time after acceleration

In other computer platforms, select the appropriate hardware and software to achieve the above algorithm in a certain way, test the calculation time. Compare the calculated data with other computer platforms to verify that the FPGA accelerates computing acceleration modules.

Contrast test using x86 processor, the international common X86 processor in China used Widely in domestic rugged computers,the contrast CPU is Core Duo L2400 dual-core. The test computer platform information shown in Table 1.

Table 1 Test platform information

Comparison items	CPU	Fequency(Hz)	Mem(GB)	OS
Loongson	3A1500	800M	4GB-DDR2	Neokylin
Loongson	3A1500 +2FPGA	800M	4GB-DDR3	Neokylin
X86	L2400	1.66G	2GB-DDR3	Rhel6.0

Each platform test comparison of running time shown in Fig. 6.

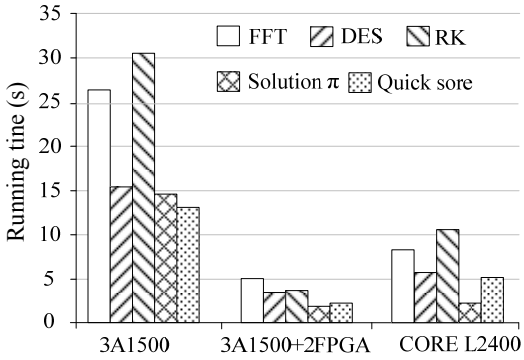

Fig. 6 Running time comparasion chart

Loongson processor 3A1500 nominal frequency of 1GHz, but found in the actual test, the stable frequency of 800MHz, so Loongson 3A1500 operating frequency of 800MHz in the test.

As can be seen from the Fig. 6, even if LS2400 dual-core processor, memory 2G case, the computing performance is still relatively good, indicating that the X86 platform computing performance. In the 800MHz operating frequency, the Loongson 3A1500 in the calculation of performance than the LS2400 obvious difference, 3A1500 +2 FPGA mode, you can greatly improve the Loongson 3A1500 computer's computing performance, acceleration than DES encryption calculation is slightly less than 5 (the algorithm needs to continue Optimization), other algorithms are more than 5, the comprehensive calculation performance is superior. Therefore, in this design, the model of Loongson 3A1500 + 2FPGA greatly makes up for Loongson 3A1500 lack of computing power. Statistics 3A1500 +2 FPGA mode for each algorithm to calculate the speedup, shown in Fig. 7.

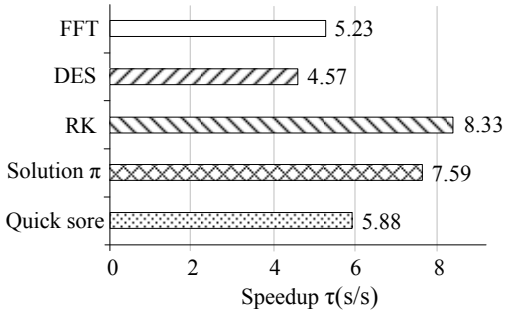

Fig. 7 Speedup comparison chart

6. Summary

This paper introduces the design method of computing acceleration module based on Loongson 3A1500, including design ideas, hardware design, software design, and finally gives the performance comparison test. The results show that the 3A1500 + 2 FPGA mode greatly enhances the overall computing performance of the Loongson 3A1500 platform with an average computing speedup of more than 5, which enhances the computational performance of the computer module based on domestic processors. The present design has a positive meaning on the development of China's fortified computers in the high-performance area.

References

[1]. Yumei Hou, Xiangdong Zhu. Warning of prism gate on network security in China. Network & computer security. (2014) No. 5, p. 33-35.

[2]. Bin Yan, HuiTao Gu. Development of domestic computer software and hardware technology. Vol. (2015) No. 8, p. 82-84.

[3]. Hui Zhao, Junwei Wan, Zhonggui Bao et al. Application of independent and controllable technology in test missions. Journal of Spacecraft TT&C Technology. Vol. 34 (2015) No. 2, p. 109-114.

[4]. Ying Wang. Loongson: security chip need Really independent & controllable. Electronic engineering & product world for engineering managers & desingers. Vol. 22 (2015) No. 9, p. 17-19.

[5]. Qiying, Liu, Yagang Liu, Shuyan Zhang et al. Reserch and application of FPGA-based hardware acceletator design. Computer CD software and applications. (2013) No. 17, p. 276-277.

[6]. Yaping. Implementation of high-speed interface between FPGA and CPU. Foreign electronic measurement technology. Vol. 32 (2014) No. 4, p. 66-68.

[7]. Information on: www.loongson.cn

[8]. Xiaonan Liu, Rongcai Zhao, Jianmin Pang. Software migration' binary translation and development of domestic processors. Journal of information engineering university. Vol. 15 (2014) No. 5. p. 613-616.

[9]. Shan Wang,Jianzhi Zhang. Design on embedded system supporting remote. Radio engineering, Vol. 44 (2014) No. 8, p. 93-96.

[10]. Jie Zhang, Naijie Gu, Ming Zhang. Vectorization study for FFT algorithm based on godson 3B. Journal of chinese computer systems. Vol. 36 (2015) No. 7, p. 1639-1643.