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Implementation of a Low Voltage Common Source Common Gate Band-Gap Reference Voltage Source with a Soft Start Circuit

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***Abstract*—This paper presents a band gap voltage reference circuit with soft start circuit design, 0.5 m 2P3M BiCMOS based on Process, and the use of low-voltage cascode current mirror structure to reduce the dependence on the voltage of the power supply, to eliminate the contradiction between precision and remaining, but also increase the soft start circuit, thus to reduce the current reference circuit at startup, protect the normal starting work circuit, and use the HL50S-S3.1S.lib library file has been simulated by HSPICE, the power supply rejection is about -78.9dB than PSRR.**

***Keywords*—Band-Gap reference; soft startup; PTAT; low voltage cascade current mirror; Bicmos**

I. INTRODUCTION

Voltage reference sources are based on voltage reference based on positive V_{BE}, voltage datum based on zener diode reverse breakdown characteristics, Band-Gap voltage reference and so on. The Band-Gap voltage reference has many advantages, such as low temperature coefficient, high power supply rejection ratio, low reference voltage and long term stability, so it has been widely used.

In this paper, the temperature level compensation method is adopted for the reference source. The so-called temperature level compensation is to select a point in the temperature region, so that the output of the reference source is zero at that point. As long as the position of this point is suitable, a smaller temperature coefficient can be obtained. The voltage is generated by a current proportional to the absolute temperature (PTAT[1]: proportional to absolute temperature). The Band-Gap adjusting circuit is dual in nature, in order to reduce the cost, and can be compatible with the CMOS[2] process, we use the BICMOS technology of 0.5um. The use of soft start circuit can better protect the work of the chip.

II. THE STRUCTURE PRINCIPLE OF THE CIRCUIT

As shown in Figure I, one end of the two resistors R1 and R2 is connected to the output terminal, and the other end is connected to the two input ends of the operational amplifier. The function of the operational amplifier is equal to the voltage of a and B two points when the circuit is in deep negative feedback. When the R3's resistance is much less than R1 and R2, we think the current of the branch is only determined by R1 and R2. When R2 = n R1, the current of the R1 branch is n times that of the R2 branch current. And the area of the Q2 tube collector is m times of the Q1 tube.

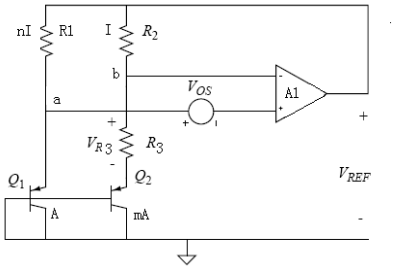

FIGURE I. TRADITIONAL BAND-GAP VOLTAGE SOURCE CIRCUIT

In the circuit of Figure I, a bipolar transistor is connected to a diode, and its emitter current can be written as:

$$I = I_S \bullet (e^{q \bullet V_{BE}/kT} - 1) \tag{1}$$

The saturated current is Is, V_{BE} is emitter positive bias voltage of the bipolar transistor, the q is the electronic charge, the k is the constant of the Boltzmann, and the T is the absolute temperature.

At that time, $V_{BE} >> kT/q$, there was $I \approx I_S \bullet e^{q \bullet V_{BE}/kT}$, so there was

$$V_{BE} = V_T \bullet \ln(I/I_S) \tag{2}$$

$$V_{EB1} = V_{EB2} + I \bullet R_3 \tag{3}$$

$$V_{EB1} = V_T \bullet Ln(nI / I_{S1}) \tag{4}$$

$$V_{EB2} = V_T \bullet Ln(I / I_{S2}) \tag{5}$$

$$V_{EB1} - V_{EB2} = V_T Ln(\frac{nI}{I} \bullet \frac{I_{S2}}{I_{S1}}) = V_T Ln(m \bullet n) \tag{6}$$

When the gain of the amplifier is large when the A, B

points of potential can be considered equal, namely the area, there are:

$$V_{EB1} - V_{OS} \approx V_{EB2} + R_3 \bullet I \tag{7}$$

V_{OS} is the input offset voltage of the operational amplifier, and the imbalance is that. If the input of operational amplifier is zero, the output voltage is not zero. Write out the expression of VREF and replace the (7) form:

$$V_{REF} = V_{EB2} + (R_3 + R_2)\frac{V_{EB1} - V_{EB2} - V_{OS}}{R_3} \tag{8}$$

$$= V_{EB2} + (1 + \frac{R_2}{R_3})\left[V_T Ln(m \bullet n) - V_{OS}\right] \tag{9}$$

If we ignore the influence of the unbalanced voltage of the operational amplifier, we can get the output voltage V_{REF} with zero temperature coefficient by choosing the size of the R2, R3 and N values properly. But in actual circumstances, the input offset voltage of the operational amplifier is present, and the offset voltage of the operational amplifier at the input end is magnified 1+R2/R3 times at the output end. And V_{OS} varies with the temperature, so the temperature coefficient of the output voltage is increased. Here we choose a large size device and carefully select the layout of the layout to minimize the imbalance and make the current of the Q1 a n times of Q2 to reduce the impact of V_{OS}.

III. THE CORE BAND-GAP REFERENCE CIRCUIT

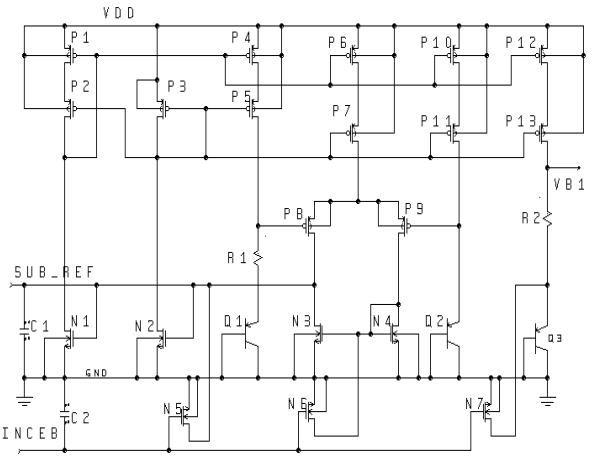

FIGURE II. ACTUAL BAND-GAP REFERENCE VOLTAGE SOURCE CIRCUIT

The actual circuit of the Band-Gap reference is shown in Figure II. R1, R2 and Q1, Q2 and op amp constitute a Band-Gap[3] reference core circuit. N5, N6, N7 are the enabling tubes. The capacitance C1 is used as the phase compensation, and the capacitor C2 acts mainly when the circuit is turned off. When CEB is leaking from low level to high power, CEB (controlled by enable module) charges C2 through signal line IN until the voltage on C2 causes N5 and N6 to turn on, then the drain voltage and grid voltage of N3 and N4 are pulled down to the ground, and the reference module stops working. A AMP_REF operational amplifier as follows: differential input stage P8, P9, N3 and N4 active load, cascode current mirror is P1, P2, P4, P5, P6, P7, P10, P11, P12, P13, they constitute a bias current source the reference module, has the characteristics of high output impedance, it the elimination of the general cascode between current mirror precision and redundancy contradiction and good stability. This is actually the cascode current mirror input and output shorted cascode structure, diode connected transistor for generating P3 cascode current mirror gate voltage, when the drain source voltage P1 and P4 constant, cascode current mirror P4, P5, P6, P7, P10, P11. P12, voltage P13 redundancy and minimum consumption, can be precisely the current mirror.[4]

IV. SOFT START CIRCUIT

This module uses bias signal VB to realize self-offset and self-starting function Band-Gap reference starting circuit. Band-Gap voltage VB1 through the gate of NVB1, control the working state of MN9. Just when the power chip, reference circuit does not start, Band-Gap voltage VB1 output low level, by MP14, after the gate circuit composed of MN8, NVB1 output high level MN9 saturation conduction, I2 C3 REF module to the capacitor charging, when the voltage on the capacitor reaches 0.842V, the REF module began to work VB1 voltage increases, reaches about 1V NVB1 goes low, the MN9 is off, to stop charging the capacitor C3, soft start finish. The relationship between I1 and I2 is determined by the ratio of the mirror image of the tube MP14 to the MP15, and the I2 has the current only in a moment. The C3 in the figure comes from the C1 of the REF module.

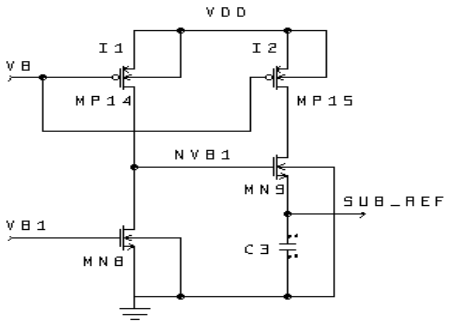

FIGURE III. CIRCUIT DIAGRAM OF SOFT START MODULE

V. SOFT START TIME SEQUENCE SIMULATION

In 40℃, 25℃, 125℃ three temperature, simulation results for reference voltage VB1 to 1.200V as follows:

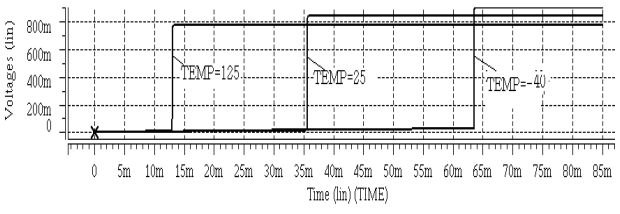

FIGURE IV. AT A TEMPERATURE OF 40℃, 25℃, 125℃, THE TIMING DIAGRAM OF THE OUTPUT REFERENCE VOLTAGE

It can be seen from the above picture that under the low

temperature [5] TT model, the charging current is smaller and the starting time will be longer. When the VREF rises to a certain level, it will turn off the charging current to the reference compensation capacitance. Here, if the threshold setting of the reverse is not reasonable, it will affect the Band-Gap reference starting characteristics. When the threshold is too low, it is too early to turn off, and the start time of the Band-Gap datum will be longer; the threshold too high will make the gap reference overcharge more serious.

VI. Noise and Frequency Characteristics

When the power fluctuates due to external disturbances, it will produce different frequency AC spectrum components. These AC components will cause a certain degree of fluctuation of the output voltage of the reference, and affect the stability of the benchmark. In this circuit, the output noise can be greatly reduced by the external 10uF Bypass capacitor, and the PSRR can be increased at the same time.

VII. Simulation of Temperature Characteristics

The supply voltage is 2.5V, 3.0V, 6.0V three, 40℃, 25℃, 125℃ to the input voltage of the scan temperature of 125 DEG C, the simulation results are shown in Figure V.

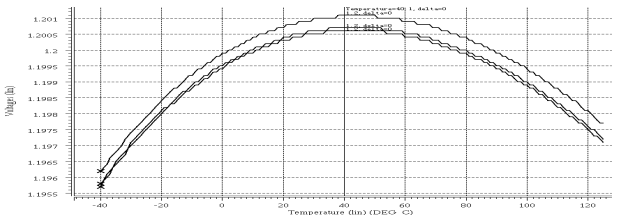

FIGURE V. THE RELATIONSHIP BETWEEN THE REFERENCE VOLTAGE AND THE TEMPERATURE UNDER THREE INPUT VOLTAGES OF MODEL=TT, 2.5V, 3.0V AND 6.0V

VIII. Simulation of Frequency Characteristic Psrr

In the case of input DC voltage 5V, we add a AC voltage of 1V, which is used to simulate noise interference, and the frequency of AC voltage is from 1 to 10MHz.

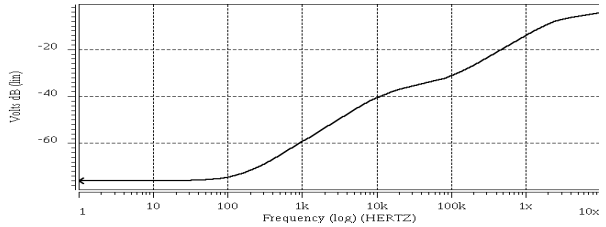

FIGURE VI. CHANGE CURVE OF POWER SUPPRESSION RATIO WITH FREQUENCY

From the diagram, we can see that in the case of 1 to 100Hz, the suppression of the power is very high. At the frequency of 100Hz, the power supply can be suppressed to -76.2dB. As the frequency increases, the power suppression decreases faster with the increase of frequency, and the power suppression ratio is -14.8dB at 1MHz. Therefore, the frequency characteristics of this circuit can meet the requirements for the low voltage differential DC voltage regulator of LDO.

IX. Conclusions

The paper presents a Band-Gap voltage source circuit with high power supply rejection ratio and temperature compensation, which uses a low voltage common source common grid current source structure. This circuit has the advantages of simple structure, low voltage, low power consumption, for the reference core circuit, the total static current as low as 2.716 uA, for soft start circuit, the static current is 0.2uA. The low-voltage cascode current mirror PMOS PTAT current, effectively reducing the channel length modulation effect, can provide a constant bias current, and the circuit can work in low supply voltage, the power supply rejection ratio can reach -78.9dB. All the indexes of the circuit have reached the requirements of the design. The circuit has good practicability and is widely used in the LDO power management.

Acknowledgment

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