

A New Neutral Point Voltage Control Strategy for NPC Three Level Inverters

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Abstract—Multi-level inverter is now becoming an efficient and promising technology in sorts of applications, especially in high level voltage inverters. However, the unbalanced voltages between two DC-link capacitors while operating the Neutral Point Clamped (NPC) three-level inverters is an inherent problem, which in a way can excessively affect the quality of the output voltage. In this paper, a new strategy for NPC three-level inverter in DC-link balancing control is proposed. The proposed strategy is implemented by both adjusting the acting time of P-type small vectors and N-type small vectors in the duration times of the nearest three vectors space vector modulation and changing the switching sequences of redundant small vectors of every switching period. These two modes are selected based on the difference value of the neutral point voltage. Hence it not only has the ability to limit the large neutral point voltage drift, but also reduced the switching loss. The proposed method is simple to achieve so that complex calculation and additional hardware circuits will not be needed. The results of simulation have shown that the strategy for balancing neutral point voltage is practical and effective.

Keywords— NPC inverter; neutral point balancing; hysteresis loop; switching sequence selection

I. INTRODUCTION

Multi-level inverter is now becoming an efficient and promising technology in sorts of applications, such as photovoltaic and wind power grid converters, electrical high level motor systems and electric car[1][2]. Among all categories of multi-level inverters, the neutral point clamped (NPC) three-level inverter, which was firstly proposed by A. Nabae in 1980, has the most popular and substantial applications. Fig. 1 shows the circuit topology of the NPC three-level inverters [3].

Compared with the conventional two-level inverters, it has the advantage of generating high-voltage while the withstand voltage of power switch devices is just half of the output voltage. Furthermore, three-level inverters have lower total harmonic distortion (THD) and reduces the dv/dt stresses on individual devices, thereby decreasing the electromagnetic interference (EMI) of the system.

As it shown in Fig. 1, the NPC three-level inverter generates different level of voltages due to the two DC-link capacitors. This issue is caused by the unbalanced charging and discharging of the two DC-link capacitors during switching cycles.

Many scholars and experts around the world have been studying this important issue in many ways for many years. Several algorithms have been proposed in the literature for balancing the neutral point voltage. Generally, the unbalanced neutral point voltage is constrained by adjusting the small vectors and medium vectors in space vector pulse width modulation (SVPWM) and injecting common mode voltage injection method (CMV) in sinusoidal pulse width modulation (SPWM) [4-8]. Nevertheless, once the neutral voltage drifts largely, the conventional modulation algorithm is hard to bring it back to the balance point.

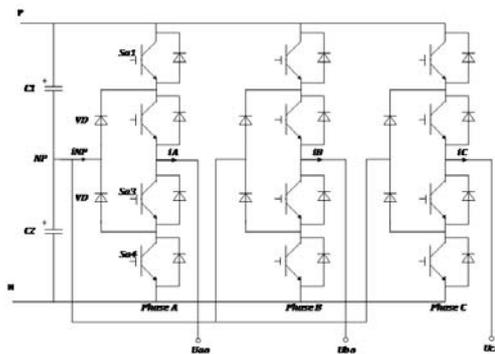


FIGURE 1. NPC THREE-LEVEL INVERTER

II. DESCRIPTION OF SVPWM FOR NPC THREE-LEVEL INVERTER

The phase leg of NPC three-level inverter can generate three kinds of voltage states (P,O or N) based on the switching states of four power devices on each leg. The switching combinations for P, O and N states is given in Table I. The three phase reference voltage V_r is calculated according to (1) and switching function (2) is introduced to replace the V_a, V_b and V_c . Hence, the modulation function V_r' for SVPWM is calculated in (3).

$$V_r = V_a + e^{j\frac{2\pi}{3}} V_b + e^{j\frac{4\pi}{3}} V_c \tag{1}$$

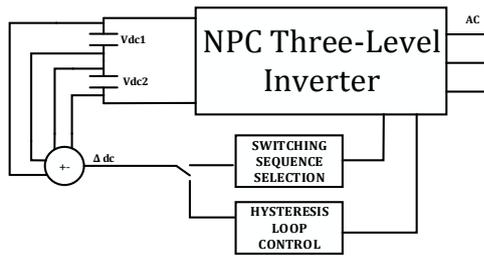


FIGURE III. SCHEMATIC DIAGRAM OF THE PROPOSED CONTROL STRATEGY

Changing the two control strategy by detecting the difference value of the two DC-link capacitors at the real time. As it shown in Fig.4, a is the changing point of the two strategy.

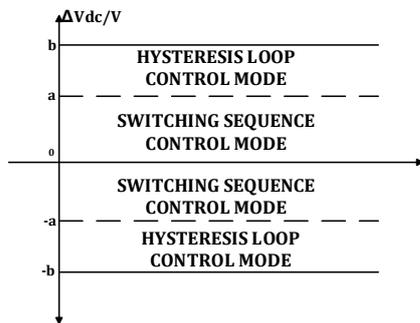


FIGURE IV. MODE CHANGING POINT

While $\Delta V_{DC} \in [-a, a]$, the switching sequence mode is selected to control the NP voltage, thereby limiting the fluctuation as long as reducing the switching loss. Furthermore, if $\Delta V_{DC} \in [a, b]$ or $\Delta V_{DC} \in [-b, -a]$, the hysteresis loop NP control mode is applied to bring the NP voltage back to balanced state.

IV. RESULTS AND CONCLUSION

The simulation of the proposed neutral point voltage strategy and SVPWM algorithm has been carried at switching frequency 10 kHz. The voltage supply is 200V and divided by two DC-link capacitor. Three phase R-L load is implemented in the simulation with 10Ω resistance and 5e-2L inductance.

Fig.5 shows that when an unbalancing state occurs between two DC-link capacitors, while $\Delta V_{DC} > 2V$, the hysteresis loop NP voltage control mode is selected to bring the drift voltage back to 0, after $\Delta V_{DC} \in [-2, 2] V$, the switching sequence mode is applied to keep the NP voltage into small scale of fluctuation. Fig.6 and Fig.7 show the line voltage and neutral point current, respectively.

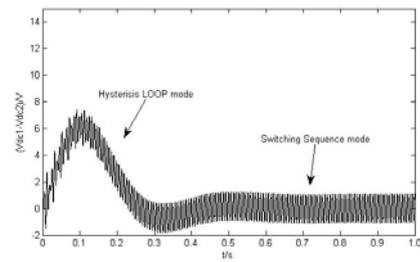


FIGURE V. EFFECT OF PROPOSED STRATEGY ON NP VOLTAGE

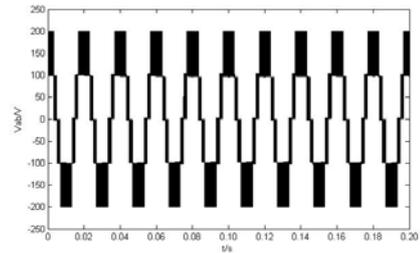


FIGURE VI. LINE VOLTAGE OF OUTPUT

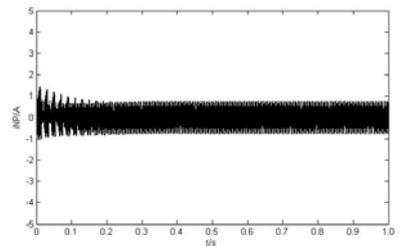


FIGURE VII. CURRENT OF NEUTRAL POINT

Results show that the proposed switching sequence selection along with hysteresis loop neutral point voltage control strategy has high controllability and strong balancing ability even if with large imbalance. Furthermore, the switching loss is reduced compared with conventional strategy.

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