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The Influence of the Distance between the Strike Location and the Drain on 90nm Dual-Well Bulk CMOS

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***Abstract*—Based on the 3D TACD simulation, by building and simulating 90nm dual-well CMOS device under heavy ion radiation with different distance between strike position and the drain, researching the influence to NMOS, PMOS, SRAM threshold LET and the critical charge. For NMOS, with the increase of the distance, bipolar amplification effect will reduce influence even make no difference. The situation in PMOS is as same as the condition of a directly strike on drain, and the bipolar amplification effect increases the charge collection efficiency. Meanwhile, as the distance increases, the threshold LET and the critical charge of SRAM while increase.**

Keywords—strike location; bipolar amplification effect; critical charge; threshold LET

I. INTRODUCTION

Heavy ion strike the sensitive area of semiconductor device under radiation environment, it will cause Single Event Transient (SET) pulse. Study [1] shows that, heavy ion strike on drain area that under the OFF state may generate transient current; the current will react with materials in radiation track. In study [2], after heavy ion enter sensitive area of CMOS device, for PMOS, the PN junction between source and N-well will positive biased. Which increased the number of charge collected by drain. For NMOS, the charge sharing mainly comes from the diffusion effect. The critical charge (Q_{crit}) and LET threshold (LET_{th}) are also one of the research hotspots. They are important parameters to measure SRAM overcome single-event upset ability. Study [3] and [4] show that the collection charge making the SRAM flip is about 1.50fC.

However, at present, most of the studies only aim at the single event effect caused by the drain zone in the OFF state of heavy ion radiation. Vanderbilt University proved that there is relationship between charge collection and radiation position to the drain [5]. According to the position of heavy ion radiation, Université de Montpellier and STMicroelectronics also proposed the concept of collection efficiency, corrected the collection-diffusion model [6]. Although they suggested that the charge collection efficiency is related to the strike location, at present, few literatures review has been conducted on the parasitic bipolar amplification effect and the Q_{crit} when the position of the hit position is well.

This paper studies the influence of the distance from the strike position to the drain on the 90nm double-well CMOS device. In Section II, the NMOS and PMOS had built and calibrated. In Section III, the paper discussed the influence due to the distance change between the drain and strike position to NMOS and PMOS respectively. In Section IV, the paper will study SRAM LET_{th} and the Q_{crit}.

II. DEVICE SIMULATION AND CALIBRATION

Based on Synopsys Sentaurus TCAD, building 3D NMOS and PMOS, as shown in figure1and figure 2, the aspect ratio of gate's width and length of NMOS and PMOS is 175nm:100nm and 100nm:100nm. By adjusting the doping concentration of the source and drain, lightly doped concentration of drain and other process parameters for calibration of two device. Calibration benchmarks is the SMIC 90nm process. The I-V characteristics of the device model and the SPICE are shown in figure 3, figure 4, figure 5 and figure 6.

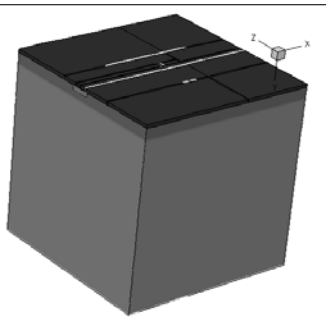

FIGURE I. PMOS 3-D DEVICE MODEL

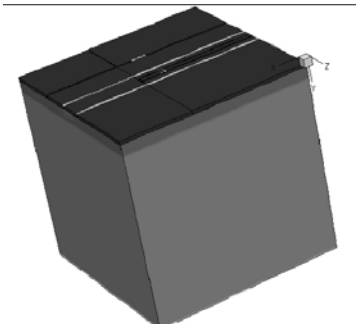

FIGURE II. NMOS 3-D DEVICE MODEL

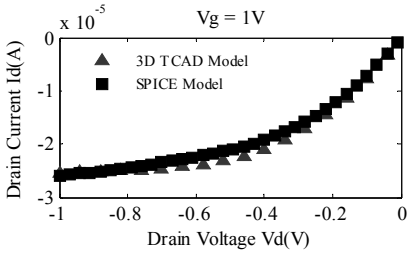

FIGURE III. PMOS PROCESS CALIBRATION ID-VDS

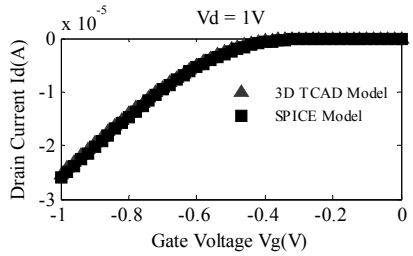

FIGURE IV. PMOS PROCESS CALIBRATION ID-VGS

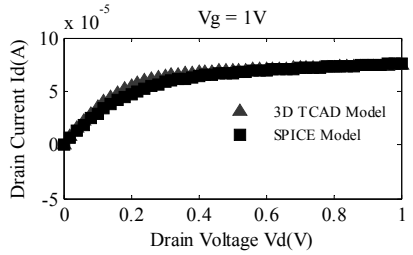

FIGURE V. NMOS PROCESS CALIBRATION ID-VDS

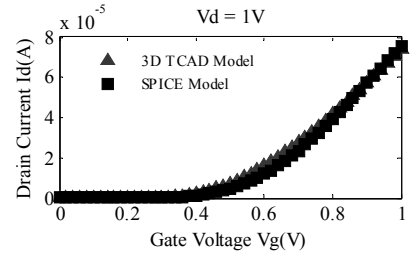

FIGURE VI. NMOS PROCESS CALIBRATION ID-VGS

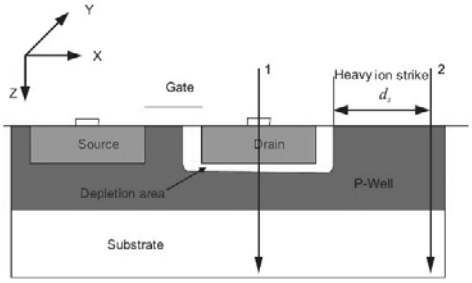

FIGURE VII. CROSS-SECTIONAL VIEW OF NMOS OF HEAVY ION STRIKE

III. Distance Between Strike Location and Drain and Parasitic Bipolar Effect

It is common to build two transistors to separate parasitic bipolar amplification effect and drift and diffusion part. The two transistors, one is normal and another one without source (referred to Diode in the following article). Compare the charge collection and the transient current formed in each transistor. Here used the same method as the paper [2], simulated the OFF state transistor SET current pulse caused by heavy ion radiation. The paper will discuss two condition when heavy ion hit the center of drain and at a distance between the drain's edge and strike location, as shown in figure 7.

A. Single NMOS Device Simulation Analysis

When LET=0.5pC/μm, the comparison result of SET current pulse of NMOS transistor under OFF state and reverse biased Diode could be simulated. As shown in figure 8, because of the existence of source, electrons quickly drift to the drain region under the effect of reverse biased Diode, leaving holes remove from the p-well by the well contact. Once the raised potential of the p-well cause the PN junction of the source/p-well is forward biased. The positive biased PN junction will attract the well electrons flow to the source, thereby increasing the current pulse height. However, NMOS drain current is mainly composed of the diffusion current, the proportion of electron current generated by the bipolar effect is small. This phenomenon is consistent with the paper [2].

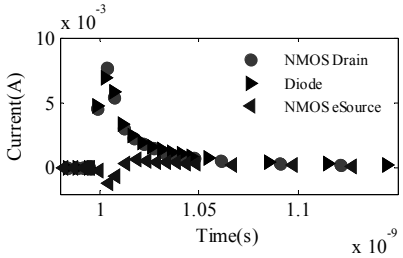

FIGURE VIII. COMPARISON OF THE CENTER OF DRAIN

The simulated current pulse width of NMOS and a reverse biased Diode remains the same when the strike position is at a distance from the edge of the drain. However, as the distance larger, the current pulse height of NMOS is less than the reverse biased Diode; the gap between two pulses becomes more and more obvious. The collection charge of NMOS when d_s is 0.2μm, 0.4μm, 0.6μm is 21.92fC, 16.23fC and 11.28fC. The Diode is 25.50fC, 18.83fC and 13.87fC correspondingly. Because as the distance increases, the impact made by bipolar amplification effect on the drain current is smaller and even not exist. Compare with figure 7 and figure 10, because of the existence of source, the electronic current drifted to drain when ion hit is immediately extracted from the source area. However, the reverse Diode does not have the source. The electron drift to drain region are temporarily retained in the moment of heavy ion implantation, so the transient current pulse in the reverse Diode is slight larger.

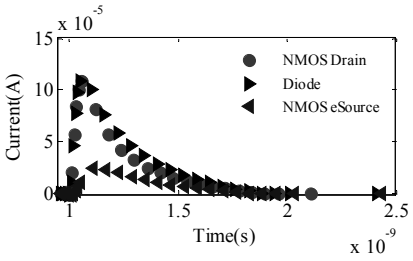

FIGURE IX. COMPARISON OF DS = 0.2MM

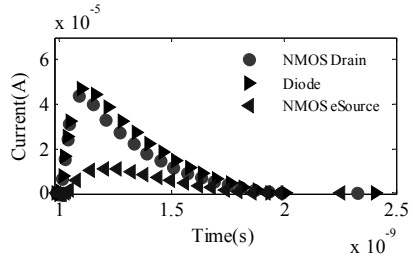

FIGURE X. COMPARISON OF DS = 0.4MM

B. Single PMOS Device Simulation Analysis

Similarly with the conditions of NMOS, Setting up LET = 0.5pC/μm, hit vertically in the center of drain. As shown in figure 11,same as the case of NMOS, because of the existence of source, the amount of deposited charge collected by the PMOS is -190.79fC (drain total current charge) and 310.85fC (source holes current charge), which is obviously much higher than that of the reverse biased Diode, whose is -90.66fC. The source acting as a PNP emitter, injects holes into the n-well (act as base), there are more holes to diffuse to and been swept in by the drain (act as collector). Meanwhile, the p-well can act as a collector in this bipolar process, too, thus, the existence of the source cause more charge collected by the p-well. However, the n-well would collects less charge, there is a large number of electrons are back-injected through the source instead of exiting through the n-well contact [7].

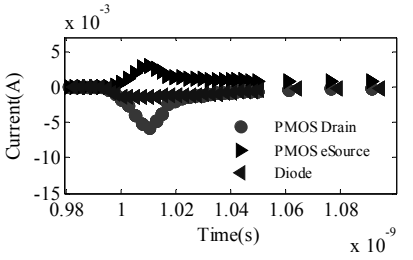

FIGURE XI. COMPARISON OF THE CENTER OF DRAIN

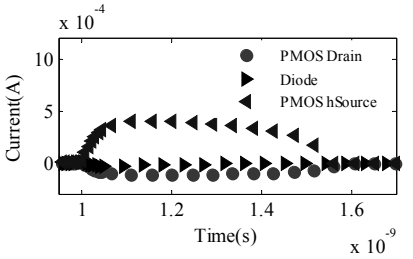

FIGURE XII. COMPARISON OF DS = 0.2MM

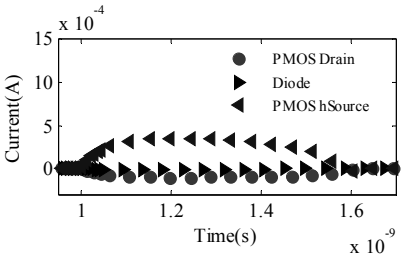

FIGURE XIII. COMPARISON OF d_s = 0.4μm

TABLE I. TOTAL COLLECTION CHARGE OF PMOS AND DIODE

Distance (μm)	PMOS Charge (fC)	Diode Charge (fC)	Percentage (%)
d_s=0	190.79	90.66	47.5
d_s=0.2	56.94	8.86	15.6
d_s=0.4	52.48	4.88	9.3
d_s=0.6	52.45	4.31	8.2
d_s=0.8	37.06	0.26	0.7

When there's a certain distance from the strike position to drain, the characters of PMOS and NMOS have large difference, and the source still have a big effect on drain current. As shown in figure 12 and figure13, as same as the condition strike vertically on drain, the existence of source still have cause parasitic bipolar amplification effect, and not discussed here. More importantly, with the strike location far from sensitive areas, charge deposited by holes drift in the drain region is less. Table 1 shows the total collection charge proportion of Diode and PMOS drain. Because of the existence of the source, bipolar amplification effect become more obvious. Most of the PMOS drain collection charge are produced by source holes. Few are came from holes drift.

IV. SRAM THRESHOLD LET VALUE AND CRITICAL CHARGE SIMULATION ANALYSIS

In a TCAD simulation of SRAM, the simulation process will be very slow to build a 3D model of whole device, and its requirement to computer is high. So using mixed simulation model on the promise of ensuring the accuracy of simulation results. The mixed TCAD simulation is shown in figure 14.

Soft Error Rates (SER) for SRAMs depend on the Q_{crit} of the circuit and the amount of charge collected by sensitive circuit nodes, so, study the trend of change of Q_{crit} along with the change of hit positions is very important for soft error rates assessment. According to the paper [8], the LET_{th} value refers to the minimum LET value for SRAMs flipping. The Q_{crit} is the minimum amount of charge needed for SRAMs flip. The formula been defined as follows, where T_f is the flipping time.

$$Q_{crit} = \int_0^{T_f} I_D(t)dt \,. \tag{1}$$

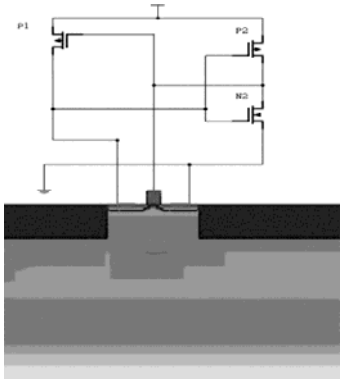

FIGURE XIV. MIXED SIMULATION MODEL

Figure 15 shows the change of drain voltage over time when the strike position is the center of the drain. When LET is greater than 0.0083 pC/μm, SRAM flipping, so, the LET_{th} is 0.0083 pC/μm. Q_{crit} is about 1.77fC according to equation 1, and the result is approximate to research result in [3] and [4].Simulating heavy ion strike on d_s 0.2μm, 0.4μm, 0.6μm, get the LET_{th} , Q_{crit} and the relationship between location of the radiation and the distance of the drain as shown in figure 16 and figure 17. Within a certain range, the LET value required by SRAM is larger with the distance increase. It is easy to understand that the ability of collecting charge is weaker for drain when it further from the sensitive area, and causing the increasing of the $LET_{th.}$ At the same time, the Q_{crit} needed for the SRAM flipping is getting bigger. When the strike distance is not in the sensitive region but well which has a distance with the drain, the effect of parasitic bipolar amplification on NMOS can hardly be ignored, as mentioned in the above section II-B. SRAM flips is the result of charge collection, and the charge collection efficiency decreases, which results in that SRAM needs more charge to make it flip [9]. Research [10] point out that when the distance is large enough, the Q_{crit} is dependent on distance. Meanwhile, the cell-flipping conditions are not dependent on the pulse waveforms as long as the pulse is a short pulse and, conversely, that long pulses have shape-dependent responses [11].From section III-A, when hit location is not the center of drain, the sharp of current is no longer a double exponential, but approximate to rectangular.

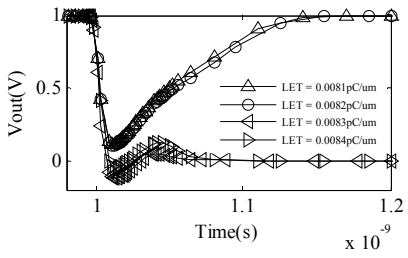

FIGURE XV. DRAIN VOLTAGE VARIATION OF DIFFERENT VALUE OF LET

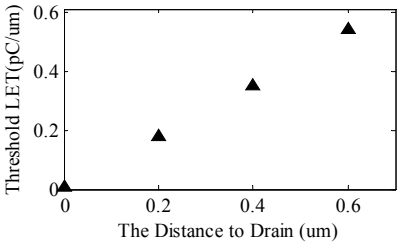

FIGURE XVI. RELATIONSHIP BETWEEN DISTANCE AND THRESHOLD LET

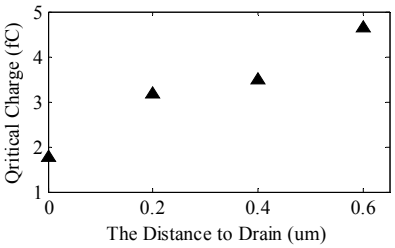

FIGURE XVII. RELATIONSHIP BETWEEN DISTANCE AND CRITICALCHARGE

V. CONCLUSION

From the paper, we concluded that strike position influence the parasitic bipolar amplification effect, SRAM LET_{th} and the Q_{crit} a lot. To be accurate, with the increase of the distance, bipolar amplification effect will have no difference on NMOS, and the charge collection efficiency will been decreased. PMOS's condition is the same as in the case of a directly strike in drain, and the parasitic bipolar effect increases the charge collection efficiency. Meanwhile, the threshold LET and the critical charge of SRAM increase obviously.

ACKNOWLEDGEMENTS

The National Natural Science Foundation of China (Grant No.1630133) and the Fundamental Research Funds for the Central Universities (Grant No.ZYGX2016J185) support this study.

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[11] Merelle T, Chabane H, Palau JM. “Criterion for SEU occurrence in SRAM deduced from circuit and device simulations in case of neutron-induced SER” [J]. IEEE T NUCL SCI, 2005, 52(4):1148-115Figure 17. Relationship between distance and critical charge