A Sample-and- Hold Circuit for a Resolution Pipelined ADC

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Abstract. A sample-and- hold circuit for a resolution pipelined ADC is presented. The circuit uses a fully differential capacitor flip structure to reduce power consumption. Increase the gain by using an olded-cascode amplifier. Based on 0.35μm CMOS process, the Hspice simulation shows that the circuit can work correctly at 3.3v power.

Introduction

The sample-and-hold (S/H) circuit plays an important role in the ADC, and is one of the key modules of the pipelined ADC[1-4]. The main function of S/H is to collect analog signals and save them until ADC completes the processing of these information[5-7]. In data conversion, the design of the S/H circuit is a very important part. Its performance restricts the speed and precision of the data converter[8,9].

The structure of the sample-and hold circuit

The structure of sample-and hold circuit can be divided into two categories: charge redistribution structure and capacitance reversal structure[1,10-12]. Figure 1 is a charge redistribution structure. In the sampling stage, the input charge is stored on the sampling capacitor, and at the holding stage, the differential charge is transferred to the feedback capacitor through the charge redistribution process. Because the input common mode charge is always on the input capacitor, so the sample and hold circuit of the structure can handle the common mode range of the input signal is large, and the performance in the single ended application is excellent.

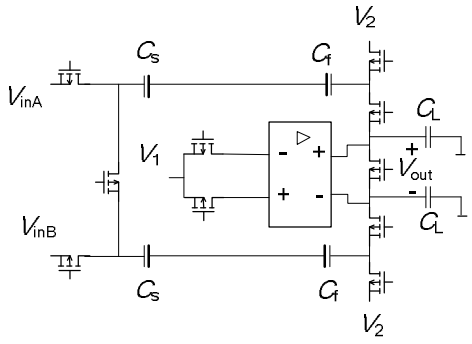

Fig.1 The sample and hold circuit of Charge-redistribution architecture

Figure 2 is a capacitor flip structure. At the sampling stage, the input charge is stored on the sampling capacitance. In the holding stage, the sampling capacitance is turned over to the output end by the switch, and the maintenance function is realized.

In the case of neglecting the parasitic capacitance, the feedback coefficient of the charge redistribution structure is 0.5, while the feedback coefficient of the capacitor turnover structure is 1.

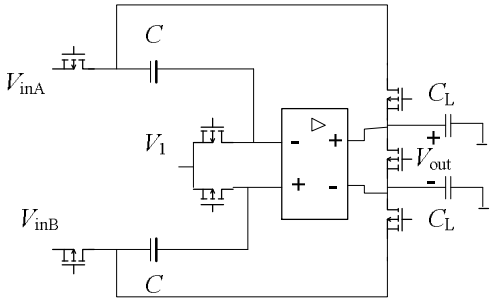

Fig.2 The sample and hold circuit of Flip-around architecture

The capacitor flip structure has 2 main advantages, first of all, it is low in power consumption. Because beta is 2 times the charge redistribution structure, therefore, in theory, under the same closed loop bandwidth, the unit gain bandwidth (GBW) of capacitor flip structure is 50% of the charge redistribution structure. This reduces power consumption. The second advantage is that the noise of this structure is relatively small.

For the consideration of noise and power consumption, this paper chooses the capacitor turnover structure. In order to be able to handle the input signals with different common mode voltages, the input common mode range of the amplifier must be increased. However, due to the existence of parasitic capacitance of the operational amplifier, the ratio of the beta of the two structures is less than 2, so the advantage of the capacitor flip structure in terms of noise and power consumption is not much larger under ideal circumstances.

Operational amplifier

The sample-and-hold amplifier is the core of the sampling and holding circuit, and its performance will directly affect the performance of the whole system.

At present, there are three kinds of common operation amplifier structure [4,13-14]: two pole operation amplifier, Cascode amplifier, and folded-Cascode amplifier. The sample-and-hold circuit uses a folded-Cascode structure. In order to improve the gain, the gain self lifting technique is used. Because of the charge injection and clock feedthrough effect will limit the application of MOS switch in the sampling circuit, the bottom plate sampling technology is adopted , so that the influence of the two effects on the circuit can be reduced effectively.

As shown in Figure 3, the gain enhanced foldable common source common gate sampling and holding operational amplifier is shown.

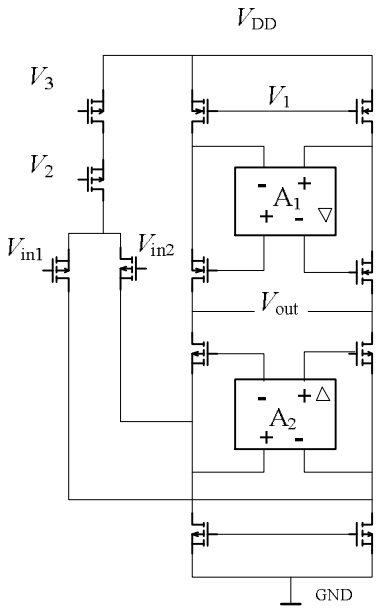

Fig.3Gain boosted folded-cascode op-amp

The input tube is the pMOS and the folding tube is nMOS. The non main poles can be extrapolated to achieve good frequency characteristics. However, using pMOS as an input tube to achieve the same speed, the size of the tube and the required current should be increased. Large size input tubes will increase the input parasitic capacitance of the amplifier. The direct consequences of this will increase the noise and power consumption. The nMOS folding tube and the pMOS current source load use the cascade structure, which will provide enough open loop gain.

A1 is the main amplifier, and the A2 is a single terminal auxiliary operation amplifier. Auxiliary operational amplifier does not affect the swing of the main operational amplifier 。

Due to the auxiliary operational amplifier introduced pole zero pair, which brought the disadvantageous influence to the establishment time of the op amp. In the design process of the auxiliary amplifiers, must make the auxiliary operational amplifier unit gain bandwidth is greater than 500MHz, to suppress the pole zero pair. However, in order to maintain the stability of the operational amplifier, the unit gain bandwidth of the auxiliary amplifier can not be too large and can not exceed 900MHz.

Simulation results and analysis

The transient characteristic of the sample-and-hold circuit is shown in Figure 4.

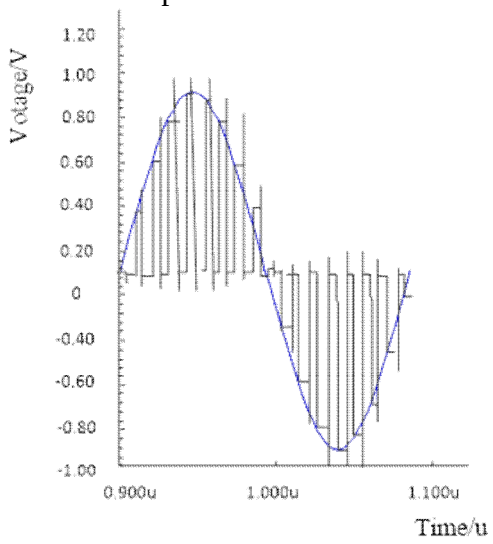

Fig.4 The transient response of the sample and hold circiut

The input signal is a sine wave of an amplitude of 1 V and a frequency of 5MHz. It can be seen that the sample-and-hold circuit can work stably. At the end of the sampling phase, the sampling value is equal to the signal at that time, and at the holding stage, the signal remains unchanged.

conclusion

A sample-and-hold circuit for pipelined ADC is introduced in this paper. Through the analysis of the structure of the sample-and-hold circuit, the capacitor turnover structure is adopted to reduce the power consumption. Through the analysis of the circuit structure of the operational amplifier, the folded-cascode operational amplifier is used to improve the gain. The simulation results show that the sample-and-hold- circuit can work steadily under the 3.3V power supply voltage.

References

[1] W.H. Yang, D. Kelly, I.i Mehr. A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-Db SFDR at Nyquist Input [J].IEEE J.Solid-State Circuits, 2001, 36(12):1931-1935.

[2]J. Arias, V. Boccuzzi, L. Quintanilla. Low power pipeline ADC for wireless LANs[J] . IEEE Journal of solidstate circuits. 2004, 39(8):1338-1340 .

[3] B. D. Sahoo, B. Razavib . A 12 Bit 200-MHz CMOS ADC [J] . IEEE Journal of solid state circuits, 2009, 44(9):2366-2380 .

[4] Y. Z. Chen, C. X. Chen, Z. M. Feng, et a1 . 14-bit 100MS/s 121mW pipeline ADC [J] . Journal of Semiconductors, 2015, 32(1):065008(1-6) .

[5]J .A . Mcneill, M. C. Coln, B. J. LARIVEE . “Split ADC” Architecture for deterministic digital background calibration of a 16-bit l-MS/s ADC [J] . IEEE Journal of Solid-State Circuits, 2005, 40(12): 2 437-2445 .

[6]P. E. Allen, D. R. Holberg, Razavi. CMOS Analog Circuit Design[M]. NEW York: Holt Rinehart and Winston , 1987.

[7] J. A. MCNEILL, M. C. Coln, D. R. Brown, et a1 . Digital background-Calibration lgorithm for “Split ADC” architecture[J] . IEEE Journal of Solid-State Circuits, 2009, 56(2):294-306 .

[8] I. Ahmed, D. A. Johns . An 11-Bit 45 MS/s pipelined ADC with rapid calibration of DAC errors in a multi-bit pipeline stage[J] . IEEE Journal of Solid-State Circuits, 2008, 43(7):1626-1637 .

[9] J. L. FAN, C. Y. WANG, J. T. WU . A robust and fast digital background calibration technique for pipelined ADCs[J] . IEEE Transactions on Circuits and Systems, 2007, 54(6):1213-1223 .

[10] Y. LIM, M. P. FLYNN . A lmW 71.5 dB SNDR 50MS/s 13 bit fully differentia ring amplifier based SAR·assisted pipelineADC[J] . IEEE Journal of solid state circuits, 2015, 50(12) : 2901-2911 .

[11] J. Zhou, L. L. Xu, F. L. Li, et a1 . A 10-bit 120-MS/s pipelined ADC with improved switch and layout scaling strategy[J] . Journal of Semiconductors, 2015, 36(8):085008(1-5) .

[12] T. Y.AGI, K. Usui, T. Matsuura, et a1 . Background self calibration algorithm for pipelined ADC using split ADC Scheme[J], Ieice Transactions on Electronics, 2011, 94-C(7):1 233-1 236 .

[13]L. Dai, J. J. Zhang. A Novel Sampling Switch Applied for 10Bits 10Ms/s SAR ADC[J]. J.NORTH CHINA UNNIV. OF TECH., 2017,29(2):28-31.

[14] Klaas Bult , Govert J. G. M. Geelen. A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain [J].IEEE J. Solid-State Circuits, 1990, 25(12):1379-1384.

[15] Y. Chiu, K. Wo .A Gain-Boosted 90-dB Dynamic Range Fast Settling OTA with 7.8mW Power Consumption [J] . IEEE Trans. Circuits and Systems □, 2003, 50 (12): 906-917.