Optimization of SRAM in 28nm HPM Technology

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Abstract. This paper presents an optimized SRAM that is repairable and consumes less power dissipation. To increase the percent of good SRAMs per wafer, redundancy logic and e-fuse box are added to SRAM, thereby building SR SRAM. In order to reduce power dissipation, power on/off states and isolation logic are introduced to SR SRAM, consequently constructing LPSR SRAM. Also the testing methodology of the SoC which has been successfully implemented Chartered 28nm HPM process is discussed. The testing results indicate that 25% of power saving is obtained to the LPSR SRAM64K×32 and the percent of the good LPSR SRAM64K×32s per wafer is increased by 20%.

1 Introduction

Embedded memories constitute a significant portion of silicon area in today's integrated circuits. Both the number of embedded memories and their average size are increasing steadily. The International Technology Roadmap for Semiconductors (ITRS) indicates that currently embedded memories occupy more than 50% of system-on-chip (SoC) area, and this number is likely to increase to 94% by the year 2014. Power consumption of embedded memories play a key role on the total power consumption of SoC and defects in memories can therefore significantly degrade the percent of good embedded memories per wafer. In such a setting, lower power dissipation and repairable embedded memories are desirable because they help reduce power dissipation of embedded memories and increase the percent of good embedded memories per wafer.

The sequel of this paper is organized as follows. Section 2 describes the optimization of Static Random Access Memory (SRAM) for increasing the percent of good SRAMs per wafer by adding redundancy logic and electric fuse (e-fuse) box. Section 3 discusses the optimization of Self Repair SRAM (SR SRAM) for less power consumption by introducing power on/off states and isolation logic. Section 4 presents the application of the Low power SR SRAM64K×32 (LPSR SRAM64K×32) in SoC, with emphasis on testing methodology and testing results are discussed in Section 5. Section 6 concludes the paper.

2 Optimization of SRAM for Increasing the Percent of Good SRAMs Per Wafer

2.1 SR SRAM block. The SR SRAM shown in Fig. 1, is an assembly of one or more SRAMs, e-fuse box and redundancy logic featuring real-time replacement of faulty memory locations. Faulty memory locations are detected during tests, their address being permanently stored into e-fuse box which is composed of many e-fuses, the number of e-fuses only depends on the memory addressing space and the number of redundant registers provided [1]. Redundancy logic, which includes Redundant Address Registers (RARs) and Redundant Data Registers (RDRs), may significantly increase the percent of good SR SRAMs per wafer [2]. For any given SRAM, the number of redundant words is calculated basing on the results of technology specific yield calculators. After power on, fault address is loaded into RARs from e-fuse box and the address at input of SR SRAM is compared with the fault address stored into the RARs. Whenever a match occurs, the redundancy logic automatically switches the data towards the word in the RDRs which are logically associated with that faulty address.

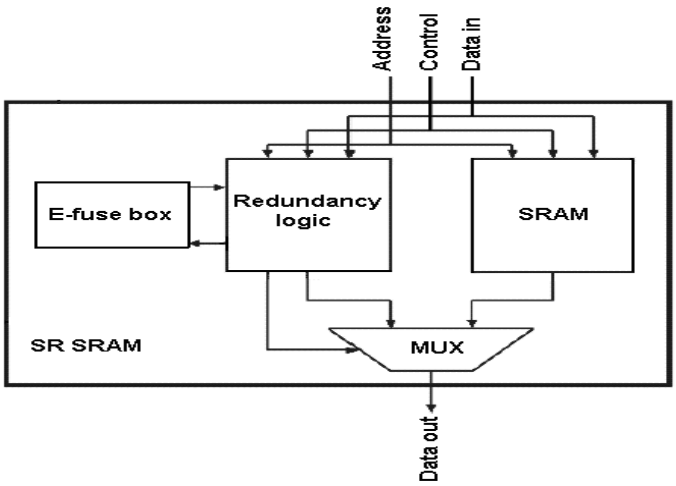

Fig. 1 Connection of SRAM, Redundancy logic and E-fuse box

2.2 Redundancy logic diagram. Fig. 2 shows the redundancy logic which consists of five functional blocks: RAR, RDR, address comparison, RDR read and RDR write. The fail signal coming from memory built-in self test (mbist) controller will go high when a SRAM faulty is deteced. Faulty address is load into RAR through rar_val_in from e-fuse box and can be output through rar_val_out for analysis. If there is no free RAR used for storing a faulty address the signal nogo will go high, this indicates that the SRAM is not repairable. Address from outside is compared with all address in RAR. As soon as a match occurs, the signal rar_match will go high and data through expected_val will write into RDR. Also a read operation will be done from not SRAM but RDR [3].

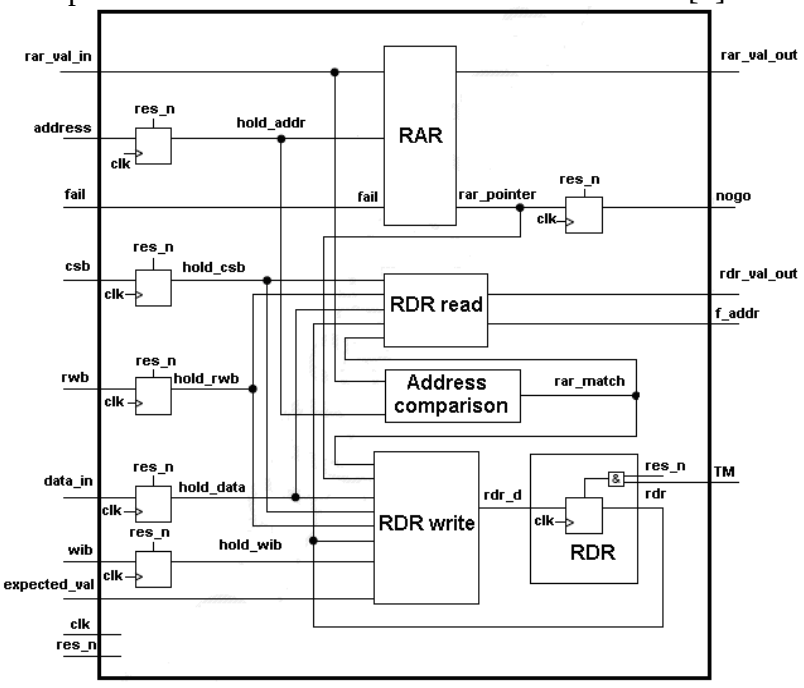

Fig. 2 Redundancy logic

2.3 E-fuse box. An e-fuse box consists of a bank of electrically programmable elements (e-fuse cells) which allow permanent storage of RAR states through fuse_val_i, programming/sensing sequences are performed by the local Control State Machine (CSM) combination with the pointer register P (see Fig. 3). E-fuses need to be sensed at every power on of the chip or the e-fuse box, RAR flip-flops are mapped one-to-one from e-fuse cells. For example, RAR element k is associated with e-fuse cell Fk. During fuse sensing, inputs clk and efw_clk must be driven by the same clock source. Signal

ready_out going active (high) for at least one efw_clk cycle indicates that fuse programming/sensing has come to completion. During fuse programming, a block of blow acceleration logic allows skipping all fuses that don't have to be programmed, thus reducing the programming time. After loading fuse states into the RAR, the e-fuse box can be electrically switched off by setting efc_isolate = 1, this allows reducing the overall leakage current of the chip [4].

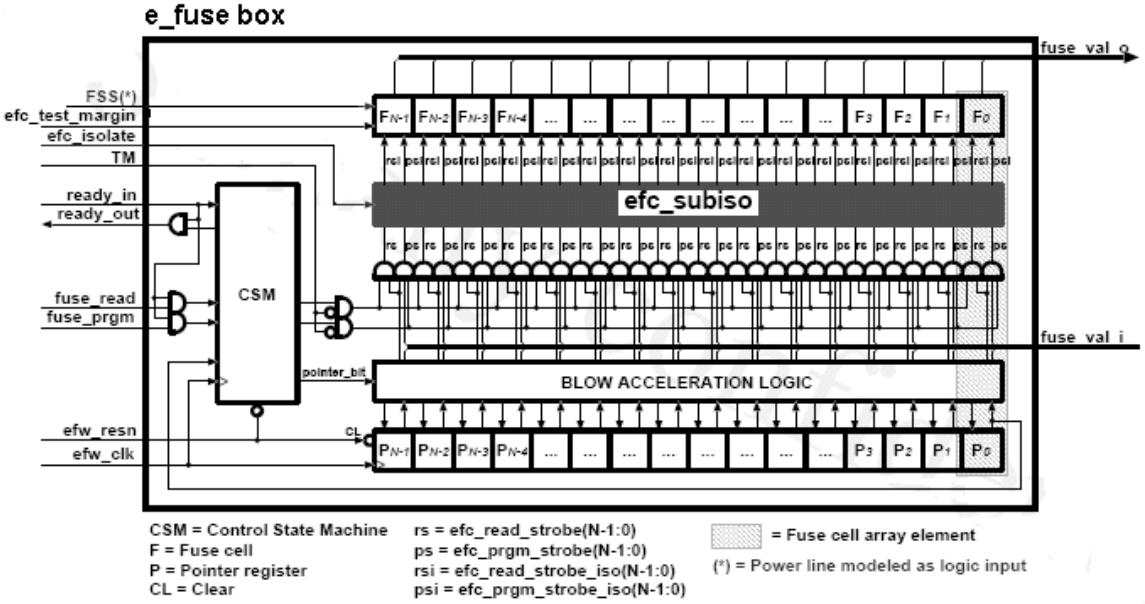

Fig. 3 E-fuse box

3 Optimization of SR SRAM for Lower Power Consumption

3.1 Power off mode. In previous SRAM, each block was in either power on state or power off state simultaneously so the power consumption was more. In our project, in order to reduce power consumption many modes of operation are introduced and each block is set in either of the states according to its actual requirement [5]. Before mbist test mode, scan test mode is done to test RARs, RDRs, e-fuses and surrounding logic. Mbist mode can be separated into debug mode and repair mode. In debug mode fault locations are detected but not repaired and the fault address is output for analysis. In repair mode, fault address is loaded into RARs from e-fuse box and the fault locations are repaired by RDRs unless there is no free RAR to be used for storing fault address. In mission mode, data are either written to or read from the memory or the redundancy logic depending on whether a match occurs between the current address and one of those stored into the RAR. When LPSR SRAM is not set in test mode, the mbist controller can be switched off. Table I shows the combinations of power on/off states in each operation mode.

Table I. The combinations of power on/off states

Mode of operation	Mbist controler	SRAM + RDR	RAR	E-fuse	Surrounding logic
Scan test mode	On	On	On	On	On
Mbist debug test mode	On	On	On	On	On
Mbist repair test mode	On	On	On	Off	On
Mission mode	Off	On	On	Off	On
Power down mode	Off	Off	On	Off	Off

3.2 Isolation logic. When a sub block of LPSR SRAM is turned off, the outputs are floated. To prevent floating lines from creating paths between VDD and VSS at the inputs of sub blocks or units to which they are connected, isolation gates are inserted to force these lines to low. Isolation logic is implemented by means of AND cells because of their input circuit structure which allows floating one or more inputs while at least one input is forced to a low state [6, 7]. In the 2-input AND circuit, a low

state at isolation control input B opens the transistor T4 and closes T2; as a consequence, voltage at node N1 which drives the inverting output stage is tied to VDD regardless of the states of T1 and T3 thus forcing output Z to a low state. In this case, no current flows through isolation gates except the total leakage current.

4 Application of LPSR SRAM64K×32 in SoC

The LPSR SRAM64K×32 which is composed of 8 blocks of LPSR SRAM64K×32 has been used in the below SoC design. Because there are many modules in our project, a test control unit, which includes mbist control logic and a finite state machine, is used to implement all testing modes [8]. In this SoC design, there are many test modes, such as mbist test mode, scan test mode, AW test mode, USB2 test mode and so on. When mbist_test_en is active (high) and the other test_ens are inactive (low), the chip will enter into mbist test mode. After entering mbist test mode, we can set mem_sel [4: 0] to select the memory which we want to test. In order to exhaustively test the LPSR SRAM64K×32 in the SoC, the redundancy logic as well as e-fuse box must be tested firstly and the test is performed by means of automatically generated scan patterns which are shifted in and out through the redundancy logic combination with e-fuse box. Then the SRAM64K×32 is scanned by a dedicated mbist controller according to the mbist algorithms implemented. As soon as an error is detected in mbist repair mode, the corresponding memory address is written into a free RAR by activating mbist_fail. If no more RARs are used to store fault address, mbist_nogo will go high and indicates that the memory is not repairable. The SoC design has been successfully implemented in a Chartered 28nm HPM process. The SoC chip occupies 10.7mm*11.9mm of die area and consumes 17.2W. The package type is FCBGA33*33 and the metal layers are composed of 10 layers of Cu. The summary of the SoC chip including the LPSR SRAM64K×32 is shown in Table II.

Table II. Summary of the SoC chip including the LPSR SRAM64K×32

Technology	28nm HPM
Package	FCBGA33*33
Metal layer	10
Supply of digital core	1.0V
Supply of IO	3.3V
Max frequency	1.2G
Pad number	205
Die size	10.7mm*11.9mm
Power consumption	17.2W

5 Testing Results and Discussion

We have tested all the 3250 SoC chips in one wafer, the diameter of which is 300mm. Each SoC chip includes one LPSR SRAM64K×32. The total power consumption equals active power combination with leakage power [9]. The result of area and power consumption of SR SRAM64K×32 and LPSR SRAM64K×32 is listed in Table III. You can easily know that the power saving of the LPSR SRAM64K×32 is (6.42-4.85)/6.42 = 25% and the area of both is nearly same because the gates

of low power logic are few. Fig. 4 is the simulation result of the LPSR SRAM64K×32 in the SoC design with ModelSim. Fig. 5 is the testing result of the LPSR SRAM64K×32 in one SoC chip with tester J750. That the Fig. 5 is coincident with Fig. 4 proves that the real circuitry in the SoC chip is coincident with that of the SoC design. Fig. 4 and Fig. 5 are all in mbist repair mode. That mbist_fail goes high for two times and mbist_nogo is always low indicates that two fault units in the LPSR SRAM64K×32 have been repaired by the redundancy logic. In mbist debug mode fault locations are detected but not repaired. Table IV is the testing summary of all the 3250 LPSR ARAMs in one wafer. After repair mode, 455 fault LPSR SRAM64K×32s have been repaired so the good LPSR SRAM64K×32s gain (%) is 455/2275 = 20%.

Table III. Area and power consumption

Memory	Voltage(V)	frequency(MHz)	Area(mm2)	Power cosumption(mW)	Power saving(%)
SR SRAM64Kx32	1.0	300	1.0	6.42	0.0
LPSR SRAM64Kx32	1.0	300	1.2	4.85	25.0

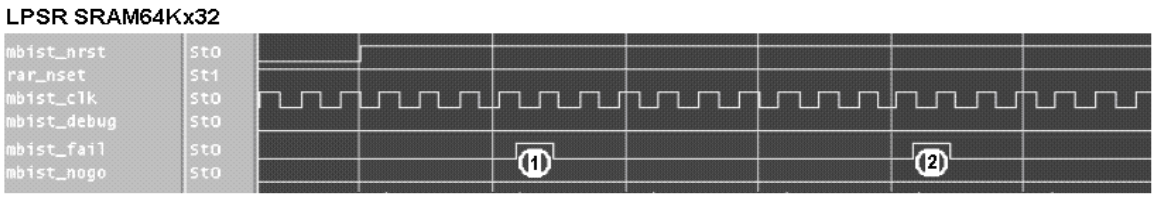

Fig. 4 Simulation result of the LPSR SRAM64K×32 in the SoC design with ModelSim

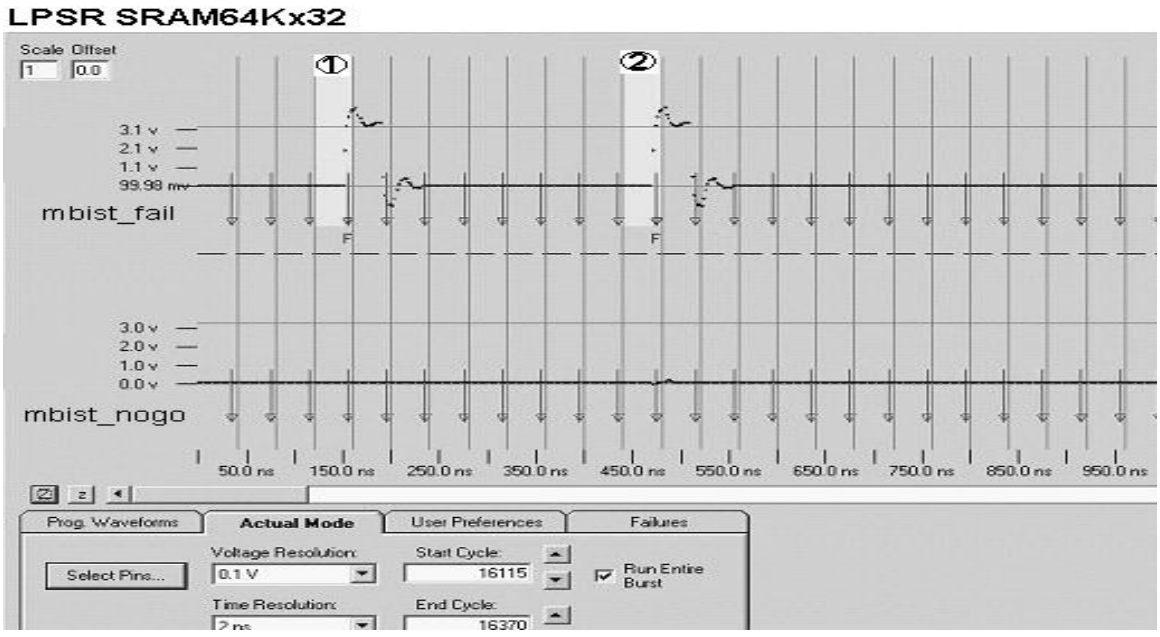

Fig. 5 Testing result of the LPSR SRAM64K×32 in one SoC chip with tester J750

Table IV. Testing summary

Mbist test mode	LPSR SRAM64Kx32s in all	Good	Repaired	Good LPSR gain (%)
Mbist debug mode	3250	2275	0	0
Mbist repair mode	3250	2730	455	20

6 Conclusions

In this paper, we have presented a new type of embedded SRAM that consumes less power dissipation with power on/off states as well as isolation logic and increases the percent of good LPSR SRAM64K×32s per wafer by means of redundancy logic combination with e-fuse box. Furthermore, the testing method of the SoC chip has been proposed. The results have proved that 25% of power saving is achieved to the LPSR SRAM64K×32 and the good LPSR SRAM64K×32s gain is 20%.

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