Design and Realization of ADC based on FPGA

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Abstract. In this paper, the signal collected by WM8731 that is a high resolution analog to digital controller (ADC) is set to establish custom NIOS II central processing unit (CPU) and peripheral controlling in the system on a programmable chip (SOPC) Builder, systems developing tool, of Altera Quartus II that is a developing software. The design and realization of ADC based on FPGA is designed, ran, compiled and simulated in Quartus II. The Design and Realization of ADC Based on field programmable gate array (FPGA) combines the advantages of embedded system and FPGA and provides a new design method of digital signal processing system of high performance. The improved method is proved to be effective.

1 Introduction

With the development of microelectronic technology, the design of electronic system is design of SOPC based on large scale FPGA instead of using various integrated circuit(IC) to carry out printed circuit board (PCB) board. At the same time, the rapid development of electronic design automatic (EDA) tools is also makes it is possible to realize the design of the whole system from the behavior algorithm level to the physical structure level implemented on FPGA[1]. And Quartus II and NIOS II introduced by Altera company provide great convenience for realizing the SOPC system based on embedded IP core of FPGA.

In this paper, the signal collected by WM8731 that is a high resolution analog to ADC is set to establish custom NIOS II CPU and peripheral controlling in the system on SOPC Builder, systems developing tool, of Altera Quartus II which is a developing software. The design and realization of ADC Based on FPGA is designed, ran, compiled and simulated in Quartus II.

2 Design and Realization of ADC based on FPGA

The signal collected by WM8731 is set to establish custom NIOS II CPU and peripheral controlling in the system on SOPC Builder based on FPGA.

The overall system block diagram of ADC based on FPGA is shown in Fig. 1.

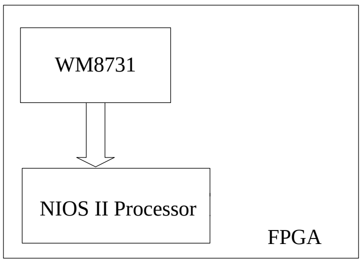


Figure 1. The overall system block diagram

2.1 Design of Hardware of WM8731 Based on FPGA.

The general ADC has 8bits, 10bits, 12 bits, 14 bits and 16 bits. In order to obtain good linearity and high resolution of the instrument, ADC with 12 bits to 16 bits are required to collect the data of signal[2]. WM8731 supports digital audio signal from16 bits to 32 bits and realizes sampling rate range 8 kilohertz to 96 kilohertz. It can directly convert the very weak input[3] signal received from the sensor into a serial digital signal without an external instrument amplifier. The WM8731 with 16 bit is used in this paper.

Design of hardware of WM8731 based on FPGA. The digital audio interface of WM8731 is the input and output interface. I2S mode, right justified mode, left justified mode and DSP mode are supported by the transmission of serial data. These modes are selected by word control. By selecting transmission mode, WM8731 is permitted to work in normal mode. The complete description of VHDL[4] is omitted according to the timing of WM8731 operating in normal mode.

Simulation of WM8731. In Quartus II [5] it is designed, compiled and emulated.

Simulation waveform of WM8731 is shown in in Fig. 2.

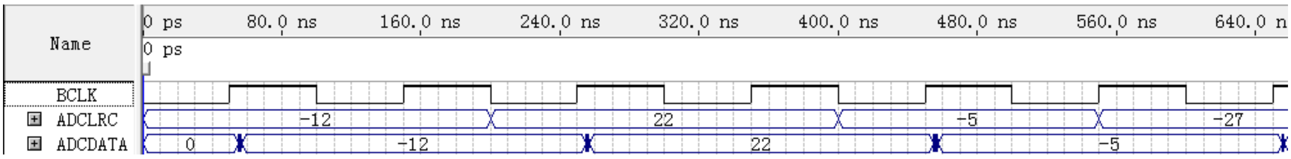


Figure 2. Simulation waveform of WM8731

The VHDL code of WM8731 is compiled and simulated in Quartus II. The simulation waveform is shown in figure 5. The results show that when the BCLK is high, the converted data, -12 , 22, -5, are output by ADCDATA. The simulation results show that the controlling conversion and output can be realized well.

The encapsulated Module Diagram of WM8731. The encapsulated module diagram of WM8731 is shown in Fig. 3.

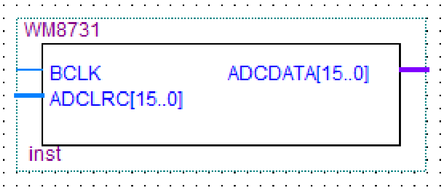


Figure 3. The encapsulated module diagram of WM8731

2.2 Design and Realization of NIOS II CPU Based on FPGA.

In this paper, the custom NIOS II central processing unit (CPU) and peripheral are established by the system on a programmable chip (SOPC) Builder, systems developing tool, of Altera Quartus II, developing software, and meet the requirements of the processor system. SOPC Builder configures embedded processing chip of high integrated SOPC system by loading NIOS II core and peripheral interfaces. NIOS II processor is a complete software development suite, including a compiler. Integrated development environment (IDE), JTAG debugger, real-time operating system (RTOS) and TCP/IP protocol stack and so on.

The hardware design flowchart of NIOS II CPU. Using powerful system developing tool of SOPC Builder of Altera and the design software, Quartus II and NIOS IDE, the design of NIOS II CPU can be completed.

The flow chart of NIOS II CPU is shown in Fig. 4.

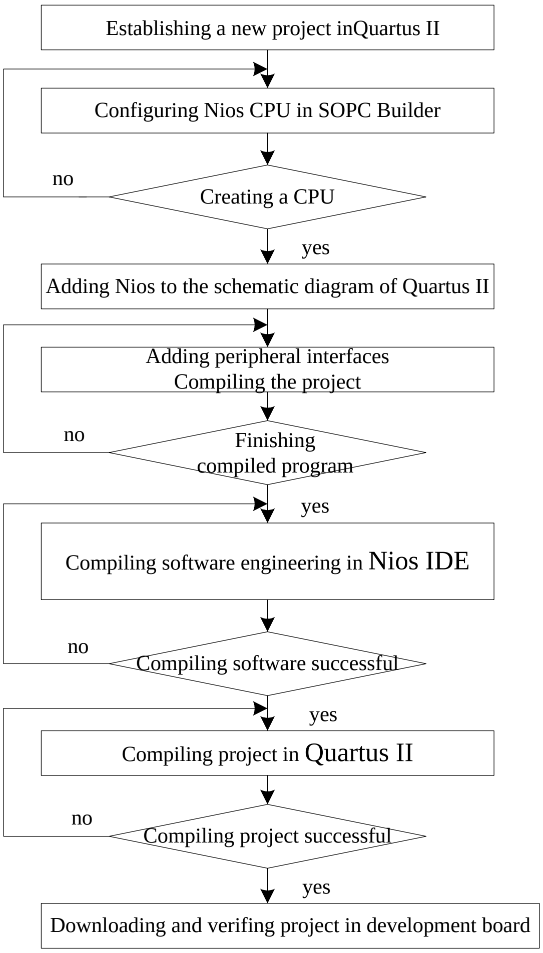
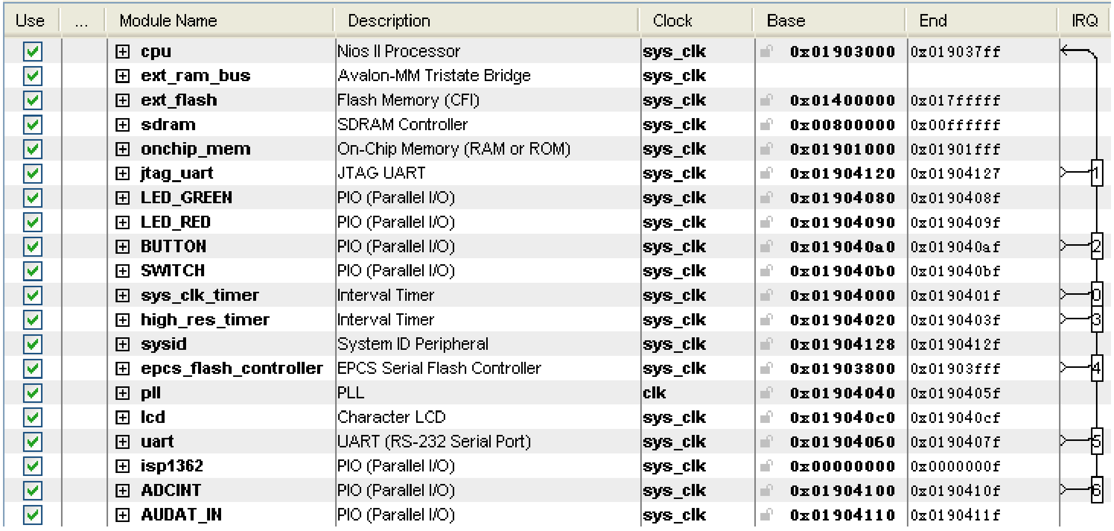

Establishing a new project inQuartus II
Configuring Nios CPU in SOPC Builder
no
Creating a CPU
yes
Adding Nios to the schematic diagram of Quartus II
Adding peripheral interfaces
Compiling the project
no
Finishing
compiled program
yes
Compiling software engineering in Nios IDE
no
Compiling software successful
yes
Compiling project in Quartus II
no
Compiling project successful
yes
Downloading and verifing project in development board

Figure 4. The hardware Design flow chart of NIOS II CPU

The design of hardware of NIOS II CPU based on FPGA. The design of hardware of NIOS II is consist of serial peripheral interface PIO, serial UART, timer, SDRAM external memory, SRAM and Flash external memory. The hardware design of NIOS II CPU mainly includes graphical user interface (GUI) and program generated by system. PTF files that describe the system are created by GUI. Each component of GUI can also provide its own configuration graphical user interface. The program generated by system generates a description of HDL for the target device. Given the limited space, the program generated by system is not listed here.

The graphical user interface is shown in Fig. 5.



Use	...	Module Name	Description	Clock	Base	End	IRQ
☑		⊞ cpu	Nios II Processor	sys_clk	0x01903000	0x019037ff	
☑		⊞ ext_ram_bus	Avalon-MM Tristate Bridge	sys_clk			
☑		⊞ ext_flash	Flash Memory (CFI)	sys_clk	0x01400000	0x017fffff	
☑		⊞ sdram	SDRAM Controller	sys_clk	0x00800000	0x00ffffff	
☑		⊞ onchip_mem	On-Chip Memory (RAM or ROM)	sys_clk	0x01901000	0x01901fff	
☑		⊞ jtag_uart	JTAG UART	sys_clk	0x01904120	0x01904127	1
☑		⊞ LED_GREEN	PIO (Parallel I/O)	sys_clk	0x01904080	0x0190408f	
☑		⊞ LED_RED	PIO (Parallel I/O)	sys_clk	0x01904090	0x0190409f	
☑		⊞ BUTTON	PIO (Parallel I/O)	sys_clk	0x019040a0	0x019040af	2
☑		⊞ SWITCH	PIO (Parallel I/O)	sys_clk	0x019040b0	0x019040bf	
☑		⊞ sys_clk_timer	Interval Timer	sys_clk	0x01904000	0x0190401f	0
☑		⊞ high_res_timer	Interval Timer	sys_clk	0x01904020	0x0190403f	3
☑		⊞ sysid	System ID Peripheral	sys_clk	0x01904128	0x0190412f	
☑		⊞ epcs_flash_controller	EPCS Serial Flash Controller	sys_clk	0x01903800	0x01903fff	4
☑		⊞ pll	PLL	clk	0x01904040	0x0190405f	
☑		⊞ lcd	Character LCD	sys_clk	0x019040c0	0x019040cf	
☑		⊞ uart	UART (RS-232 Serial Port)	sys_clk	0x01904060	0x0190407f	5
☑		⊞ isp1362	PIO (Parallel I/O)	sys_clk	0x00000000	0x0000000f	
☑		⊞ ADCINT	PIO (Parallel I/O)	sys_clk	0x01904100	0x0190410f	6
☑		⊞ AUDAT_IN	PIO (Parallel I/O)	sys_clk	0x01904110	0x0190411f	

Figure 5. The graphical user interface

Realization of NIOS II CPU based on FPGA. The hardware circuit of NIOS II is big and leaved out. Its input ports are described simply as follows.

```
clk: in std_logic;
Reset_n: in std_logic;
In_port_to_the_ADCINT: in std_logic;
In_port_to_the_AUDAT_IN: in std_logic_vector(15 downto 0);
In_port_to_the_BUTTON: in std_logic_vector(2 downto 0);
```

3 Design and Realization of ADC Based on FPGA

Using schematic input design method, the completed WM8731 and NIOS II CPU are taken as components of bottom design and encapsulated, then the top design, the design and realization of ADC based on FPGA, is finished in the edit window in Quartus II . It is realized as follow：

```
u1:WM8731 PORT MAP (BCLK=>clk,ADCDATA=>in_port_to_the_AUDAT_IN);
u2: NIOS II 81 PORT MAP (clk => BCLK, in_port_to_the_AUDAT_IN => ADCDATA);
```

Design and Realization of ADC Based on FPGA is well finished by Schematic design input method. As the hardware circuit of ADC Based on FPGA is too big, it can not be presented clearly and is omitted .

4 Conclusions

Quartus II provides a complete multi-platform design environment and is a comprehensive system design environment. Quartus II combining with SOPC Builder and NIOS II IDE provides a complete SOPC solution, makes designer to develop system conveniently and reflects the outstanding advantages of EDA tools in the designing system. The improved method is proved to be effective.

Acknowledgment

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References

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