ATLANTIS PRESS

Advances in Intelligent Systems Research, volume 143

2nd International Conference on Applied Mathematics, Modelling and Statistics Application (AMMSA 2018)

Study on Test Generation Method for Analog Circuit Board Based on Rough Set

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***Abstract*—In order to improve the repair and maintenance efficiency for analog circuit boards of certain equipment, a test and diagnosis system was designed based on virtual instrument. System structure is introduced briefly. As the key technique of the system, stimuli generation is studied emphatically. Fault simulation method based on SPICE is introduced firstly. Then test analysis and generation method based on rough set is interpreted on the basis of fault simulation. By decision table matrix reduction, test points are optimized, and fault diagnosis strategy is designed. Moreover, the AND-THEN rules generated by rough set are used in circuit fault detection and isolation. Application proves that the system has high efficiency and precision.**

Keywords—virtual instrument; fault simulation; diagnosis strategy; rough set

I. INTRODUCTION

Circuit board is the basic unit of navy warship equipment. The maintenance of circuit board plays an important role in navy equipment technique support. As circuit boards have become increasingly dependent on complex electronic systems, the necessity of testing them to ensure reliable performance has increased in a similar fashion. It is estimated that testing presently accounts for 30-50% of an electronic manufacturer's cost for a product. This percentage, in fact, actually fails to show the true cost of testing for many systems, because it ignores the cost of maintenance efforts. The repair and test for circuit boards of certain equipment are accomplished by technicians with help of normal instrument. In this course, there are many defects such as time asynchronous, effect of human factors, low efficiency, etc. Because of various test items, technician must have adequate experience. A test and diagnosis system is designed based on virtual instrument.

As the key technique of the system, stimuli generation is studied emphatically. Fault simulation method based on SPICE is introduced firstly. Then test analysis and generation method based on rough set is interpreted on the basis of fault simulation. By decision table matrix reduction, test points are optimized, and fault diagnosis strategy can be designed. Moreover, the AND-THEN rules generated by rough set can be used in circuit fault detection and isolation.

Compared to traditional test method, our test and diagnosis system can fulfill the test course automatically with shorter development cycle and lower cost of research. Application proves that the system has high precision, good operability, and high intelligence. With the system, we can ensure the exertion of battle effectiveness adequately.

II. SYSTEM COMPOSITION AND FAULT SIMULATION

A. Test and Diagnosis System Composition

This system takes LabWindows/CVI as software development platform. Compared to other software platforms, the integrated development environment, interactive programming method, function panel and abundant function library enhance its function greatly [1]. Especially, with the aid of its signal processing capability in advanced analysis library, we can analyze and process acquired data expediently.

Our circuit board test and diagnosis system is made up of multifunction data acquisition (DAQ) device, GPIB devices (signal generator and oscillograph) and master computer. It realizes test and diagnosis for circuit boards by fault diagnosis system. The composition diagram of the system is shown in Fig1.

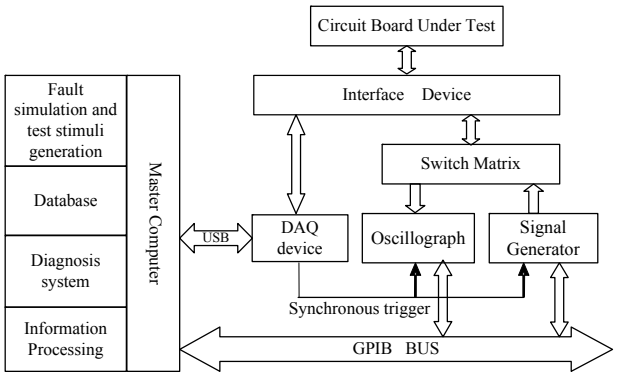

FIGURE I. SYSTEM COMPOSITION DIAGRAM

B. Fault Simulation and Test Stimuli Generation

A fault modeling method of physical fault of basic element and functional fault of integrated circuit is proposed and a technology based on PSPICE for fault modeling of simulation of analog circuit is discussed in [1][2]. In [3][4][5], The general process of analog circuit fault knowledge acquisition by fault simulation was summarized. We get the analog stimuli for diagnosis system by fault simulation. The test generation diagram is shown in Fig.2.

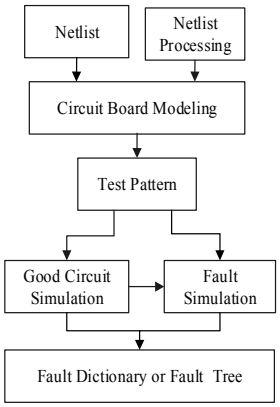

FIGURE II. TEST GENERATION FOR ANALOG CIRCUIT BOARD

Our fault simulator is developed on the basis of SPICE 3 simulation engine. The method of auto-acquiring knowledge was described in brief. The scheme of universal analog circuit fault knowledge acquisition flat was proposed. This flat could auto-enumerate all possible faults of circuit, simulate them by using external circuit simulator, extract and simplify the fault knowledge from the experiment result, and then form the structural fault knowledge basement.

Each component is defined by a set of nominal device and model parameter attributes, as well as parametric tolerances. Each component also has a set of associated failure modes. We edit the predefined failure modes or add our own catastrophic or parametric failure modes. Failure modes simulated programmatically generate the proper SPICE 3 syntax to describe the failure. Failure modes can be setup for primitive (resistor, transistor, etc.) as well as subcircuit elements. Any node on a part can be shorted to any other node, opened, or stuck [6][7]. Partial failure modes are shown in Table I. Other failure modes modeling methods are similar. For subcircuit elements, we define their failure modes in subcircuit model library.

TABLE I. SPICE3 SYNTAX FOR SOME FAILURE MODES

Fault	**Before Fault Injection**	**After Fault Injection**
Open Resistor	R9 4 5 30K	R9 4 5 100 MEG
Short Resistor	R9 4 5 30K	R9 4 5 .1
Open Capacitor	C1 11 12 10U	R_C1 11 12 100MEG
Short Capacitor	C1 11 12 10U	R_C1 11 12 .1
Open Inductance	L1 20 21 10M	R_L1 20 21 100 MEG
Short Inductance	L1 20 21 10M	R_L1 20 21 .1
Shorted Base Emitter	Q1 12 19 24 2N1893	Q1 12 19 24 2N1893 Rshort_19 19 24 .1
Low Beta Parametric fault	Q1 12 19 24 QN2222 .MODEL QN2222 NPN AF=1 **BF=105** BR=4 CJC=15.2P CJE=29.5P…	Q1 12 19 24 Q1_Fail .MODEL Q1_Fail NPN AF=1 **BF=10** BR=4 CJC=15.2P CJE=29.5P…
Resistor Stuck 2V below Vcc	R1 6 0 1K	R1 6 0 1K Rstuck_6 6_Stuck 6 10.00000 Bstuck_6 6_Stuck 0 V= Vcc- 2

Fault simulation includes three steps: fault modeling, fault collapsing and fault injection. We select faults and inject them into circuit model with fault modeling and fault collapsing techniques. Then, analog stimulus is applied to the circuit and its response is recorded.

The simulation results for each failure are input into integrated database. They constitute the fault dictionary or fault tree, which are used in our test and diagnosis system.

C. Fault Simulation Data Analysis

Fault simulation data of each test point obtained as a vector. Its main features are:

(1) The characteristics and dimensions of each Vector are different. They cannot be normalized to the space to handle the hyper sphere.

(2) The number of concentrated vector is variable.

(3) There may be more vectors that can be classified or repetitive, but the class center is randomized. There may be sparser in the spatial distribution, self-contained class vector.

(4) Prior knowledge about the shape of class may be obtained, but the prior knowledge of class distribution cannot be obtained.

(5) The data of a dimension may be very close, even identical;

(6) The number of class classified may be big, but less data available.

We can see that the classification used must have a pattern search capabilities, greater flexibility, for outliers and noise insensitive. Taking above problems into account, this paper applies rough set to emulation information classification, analysis and evaluation test.

III. TEST GENERATION BASED ON ROUGH SET

Rough set theory was put forward by Polish mathematician Z. Pawlak in 1982 [8]. It use known knowledge to characterize the imprecise or uncertain knowledge (approximately). The most significant difference between rough set and other theories in dealing with the problem of uncertainty and imprecision is

that it does not require any prior information. So of the problem or the procession of uncertainty can be described more objectively.

A. Rough Set Theory

An information system is the basic vehicle for data representation in the rough set framework. It is a single flat table in this context, either physically or logically in form of a view across several underlying tables. We can thus define an information system in terms of a pair <U, A>. U is a non-empty finite set of objects and A is a non-empty finite set of attributes.

$$S = < U, A, V, f > \tag{1}$$

The corresponding information generated by the domain of information systems is the test signal for the C of condition attributes. Test generation is the process of rough set attribute reduction and classification problems essentially.

B. Discernibility Matrix and Discernibility

In (1), $|U| = n$, the discernibility matrix of S is $n \times n$. A transparent method to find the core and reduces of an information system S via discernibility matrix was given in [9]:

$$\alpha(x, y) = \{a \in A \,|\, f(x, a) \neq f(y, a)\} \tag{2}$$

For each attribute $a \in A$, we denote a Boolean variable "a". If $\alpha(x, y) = \{a_1, a_2, \mathrm{L}\ , a_k\} \neq \phi$, then denote a Boolean function $a_1 \vee a_2 \vee \mathrm{L}\ \vee a_k$, which is illustrated by $\sum \alpha(x, y)$.

If $\alpha(x, y) = \phi$, then a Boolean constant is denoted to 1. Define discernibility by

$$\Delta = \prod_{(x,y) \in U \times U} \sum \alpha(x, y) \tag{3}$$

C. Information Discretization

Fault simulation results are processed discretely, with the symbols of each discrete conditional attribute (i.e., test signal) of the segment values[10][11]. The natural number i ($1 \le i \le n_i$) represents the test signal segments after reduction. Then decision table matrix is obtained and expressed by matrix K'. The rows of K' are the measured values of the test points with a fault mode (the number of representatives of the natural sub-test signal); the columns are measurements of a test signal with all failure mode.

Discretization of continuous attributes is the process of breakpoint on the attributes with the process of space division. There are equidistant partition method, such as equal frequency partition, Navie Scaler, SemiNavie Scaler, logical reasoning and other heuristic algorithms.

In this paper, a heuristic algorithm for constrained discrete constrained is put forward. It can be summarized as three steps:

(1) The minimum resolution of test signal distance is taken as constraints, which is used to calculate candidate cut set.

(2) The importance of candidate cuts is measured through some heuristic method, and selects a subset as small as possible according to measurement results from the candidate cut set, which is used as practical discrete cut set.

(3) Cut set is applied in decision table and the actual information system is discretized.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

A pulse peak demodulation circuit is illustrated in Fig.3[12]. Port 2 and port 6 of U1, port 6 of U2, port 2, port 3 and port 6 of U3 are selected as test points. As shown in table II, 38 hard faults of resistor, capacitor, diode, triode and op amp, 17 typical soft faults are simulated. In figure 1, PULSE is pulse signal (test stimulus) with cycles 1ms, pulse width 4μs, peak 0.5V. OFF is pulse signal with cycle 1ms, pulse width 90μs, peak 5V.

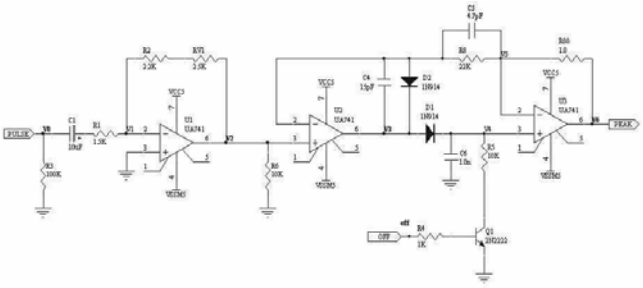

FIGURE III. A PULSE PEAK DEMODULATION CIRCUIT

TABLE II. FAULT LIST

Fault	Fault list	Number
open	R1/R2/R3/R4/R5/R6/R7/R8/R88/RV1/C1/C4/C5/C6/D1/D2/Q1_C/Q1_B/Q1_E	19
short	R1/R2/R3/R4/R5/R6/R7/R8/R88/RV1/C1/C4/C5/C6/D1/D2/Q1_BE/Q1_CE/Q1_BC	19
Parameter Drifts	R1/R2/R3/R4/R5/R6/R7/R8/R88/C1/C4/C5/C6/U1/U2/U3/Q1	17

Finally, signals are induced, and decision table matrix K is generated, as shown in Table III. In the example, K' is a

55×14 dimensional matrix. When induced, a 55×12 dimensional matrix K is obtained. In order to easy to understand, a 8×12 dimensional sub-matrix is selected for analysis.

TABLE III. PART OF DECISION TABLE MATRIX

	V1	V2	V3	V4	V5	V6	V1a	V2a	V3a	V4a	V5a	V6a
no fault	1	1	1	1	1	1	2	4	2	1	1	1
R1 short	1	1	1	1	1	1	3	1	1	1	1	1
R1 open	1	1	1	1	1	1	3	1	1	1	1	1
RV1 short	1	1	1	1	1	1	1	3	1	1	1	1
RV1 open	1	3	3	3	3	3	3	2	1	1	1	1
R2 short	1	1	1	1	1	1	1	3	1	1	1	1
R2 open	1	3	3	3	3	3	3	2	1	1	1	1
U1 Parameter Drifts	1	2	2	2	2	2	2	5	3	1	1	1

The relationship between fault and each test (conditional attributes) is described in decision table matrix. The testability modeling is finished when decision table matrix is generated.

By decision table matrix reduction, test points are optimized, and fault diagnosis strategy can be designed [13]. From Table III, we can see that decision table matrix is multivalued. Diagnosis strategy design algorithm based on extended multivalued dependency matrix can be used [14]. Moreover, the AND-THEN rules generated by rough set can be used in circuit fault detection and isolation. Aided by fault probability, testability analysis is achieved. In this example, 52 faults can be detected in decision table matrix.

V. CONCLUSION

In order to improve the repair and maintenance efficiency for circuit boards of certain equipment, a test and diagnosis system is designed. As the key technique of the system, a testability modeling and test generation method is put forward based on fault simulation and rough set. The testability information generated through fault simulation is processed with limitative and developmental discretization. Then, conditional attributes are reduced by rough set. And moreover, decision table matrix is provided. By decision table matrix reduction, test points are optimized, and fault diagnosis strategy can be designed. Moreover, the AND-THEN rules generated by rough set are used in circuit fault detection and isolation. Application proves that the system has high efficiency and precision.

ACKNOWLEDGMENT

This work is supported partly by the Twelfth Advanced Research Project under Grant No. 51319040102.

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