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Research on High Precision Time Synchronization Scheme of Power System Based on Network

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***Abstract*—The communication network of wide-area stable control in power system requires high precision of time synchronization. At present, substations are all configured with satellite receivers to realize time synchronization, and ground network has not been realized yet, which has a large potential safety hazard. In order to achieve high-precision clock synchronization on the network in power system, this paper proposes to build the main standby time synchronization system in the station with GPS and Beidou, and implement the time synchronization between stations by IEEE-1588 protocol, so that a three redundant time synchronization system is formed with GPS, Beidou and network. A high precision time synchronization scheme based on network is implemented to meet the high accuracy and reliability requirements of wide area measurement in power system.**

Keywords—time synchronization; IEEE-1588; wide area stability control

I. INTRODUCTION

In recent years, with the rapid development of power grid, cross-regional power grids have put forward higher requirements for protection and control functions. The real-time collection and transmission of wide-area information has increasingly become a bottleneck restricting the safety and stability control capacity and efficiency of large-scale power grids. Therefore, the information and communication system which can meet the demand of real-time data transmission and has wide area security is the basis for realizing intelligent analysis of large power grid and the coordinated control of wide area stability. [1] In the wide-area stability control communication network, time is an important attribute, for the time synchronization precision can have a serious impact on the stable control service.

In China's power system, timing sources are mostly GPS systems, Beidou systems, or GPS and Beidou mutual backup systems. GLONASS systems, television clock systems, and radio timing systems are basically not used. When using GPS or Beidou system, the satellite receiver needs to be configured to receive time signals, and is limited to a single substation. to realize synchronization, without achieving unified timing between stations. [2]In terms of timing mode, the most widely used method is the B code mode, pulse mode, serial port mode and network mode are used, but the proportion is very small. In general, the time synchronization between the substations is achieved by configuring satellite receivers, and the ground networking has not been realized yet. Because the safety and reliability of satellite positioning system are susceptible to environmental factors, there is a large safety hazard, and the existing transmission network of power system cannot meet the precision requirements of the differential protection for the regional protection control system without precise timing solution for phase. In addition, the synchronization interface of the service equipment or system that requires time synchronization is also inconsistent. [3] Therefore, in order to solve the above problems, it is necessary to study the synchronization clock that satisfies the accuracy and reliability requirements of the power system.

In view of the urgent need for high-precision clock synchronization on the network of wide-area measurement in power systems, many scholars have carried out researches and put forward valuable solutions. For example, the GPS second pulse and high precision crystal vibration are combined to produce high precision clock by using the complementary characteristics of the two errors. [4] In recent years, network timing technology based on IEEE-1588 protocol has also been widely studied, and there have been a few applications. The IEEE-1588 protocol can expand the scope of unified timing, making up for the inability of the clock device based on satellite receivers to realize the timing between stations. With the emergence of the IEEE-1588 protocol, the distributed system based on Ethernet achieves accurate synchronization.

This paper focuses on the lack of wide area time synchronization in power system and the reliability of satellite based time synchronization. By analyzing the time synchronization principle of IEEE-1588 protocol, the characteristics and effects of network synchronization protocol are studied. This paper proposes a technical plan to build time synchronization system of inter host-standby station based on GPS and Beidou with IEEE-1588 protocol to realize time synchronization between station The system has the characteristics of high synchronization precision, good reliability and wide applicability, which can meet the requirements of high-precision network synchronization for wide-area measurement in power systems.

II. INTRODUCTION TO IEEE-1588

A. Technical Overview of IEEE-1588

The IEEE 1588 Precision Time Protocol (PTP) is a comprehensive solution based on Ethernet to realize precise time synchronization. For the smart grid requiring higher time precision, the IEEE1588 standard precise time protocol

conforms to the trend of message synchronization. It draws on the NTP technology and can implement related services based on the PTP protocol stack.

An IEEE 1588 Precision Clock system includes multiple nodes, each representing a clock, connecting via a network. In the network, each clock may be in three states: SLAVE, MASTER, and PASSIVE. [5]The state of each clock is determined according to the optimized clock algorithm, and the three-layer structure of IEEE1588 changes with the network structure.

B. Synchronization Principle of IEEE-1588

The IEEE-1588 protocol uses the principle of ping-pong timing, which calculates the delay of the line and the time difference between nodes by the time mark of the message sending and receiving time. In the protocol of V2 version, the terminal device is divided into the master and slave according to the logic function, and P2P and E2E timing mechanisms are defined. [6]The former uses a point-to-point straight-through timing mechanism, while the latter uses end to end, segmented and step by step timing mechanism The mechanism of P2P can be applied to the network structure with complex topology and numerous nodes, while E2E is suitable for network structure with simple topology and few nodes.

In E2E mode, the calculation of line delay and time difference between nodes is shown in Figure 1.

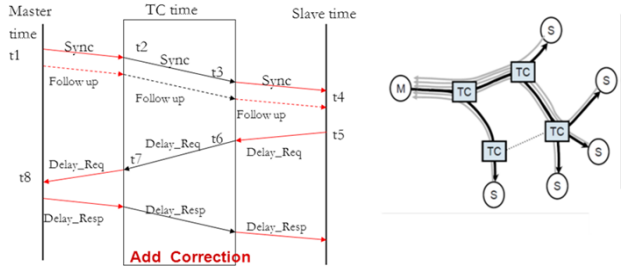

FIGURE I. DIAGRAM OF TIME DELAY CALCULATION IN E2E MODE

As is shown, the formula for calculating the line delay and clock error in E2E mode are as follows:

$$Delay= [(t4-t1) + (t8-t5) - (t3-t2) - (t7-t6)]/2 \quad (1)$$

$$Offset= [(t4-t1) –(t3-t2)] -Delay \quad (2)$$

In P2P mode, the calculation of line delay and time difference between nodes is shown in Figure 2.

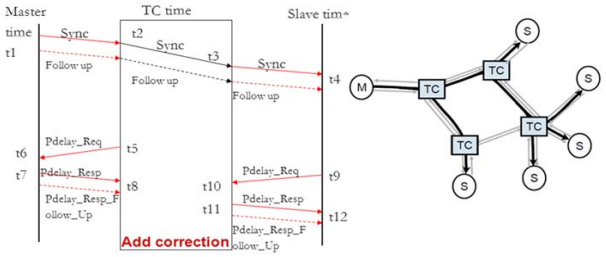

FIGURE II. DIAGRAM OF TIME DELAY CALCULATION IN P2P MODE

As is shown in the diagram, the formula for calculating the line delay and clock error in P2P mode are as follows:

$$Delay=[(t8-t7) –(t4-t3) +(t12-t11)-(t10-t9)]/2 \quad (3)$$

$$Offset= [(t4-t1) –(t3-t2)] -Delay \quad (4)$$

The comparison between IEEE-1588 and other timing modes is shown in Table 1 below.

TABLE I. COMPARISON OF DIFFERENT TIMING METHODS

	GPS	***NTP***	***Beidou***	***Atomic clock***	***IEEE -1588 v2***
Typical timing accuracy	20ns	10ms	100ns	10ns	100ns
Need satellite coverage	No	No	Yes	No	No
Locking time	40s	30ns	60s		60ns
Composite cost	Medium	Low	High	High	Low
Support Ethernet ports	No	Yes	No	No	Yes
Controlla -bility	Low	High	Medium	High	High
Security	Low	Low	High	High	Medium
Reliability	Medium	High	Medium	High	High

As can be seen from the above table, compared with other timing mode, the IEEE-1588 can achieve a better balance between precision, reliability, security and comprehensive cost.

III. DESIGN PRINCIPLE

In view of the lack of wide area time synchronization in power system and the reliability of satellite based time synchronization, this paper proposes a technical plan to build time synchronization system of inter host-standby station based on GPS and Beidou, and uses the IEEE-1588 protocol to realize the time synchronization between stations, so that a three redundant time synchronization system is formed in GPS, Beidou and network. It is suitable for synchronization in SDH networks. The overall structure diagram of the timing system is shown in Figure 3.

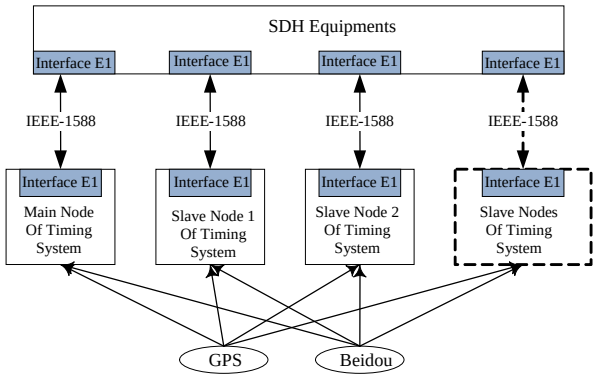

FIGURE III. STRUCTURE OF TIMING SYSTEM .

A. *Instation Synchronization Technical Scheme*

In the substation, the whole station is equipped with two time synchronization devices, one main and one standby. The clock device can receive GPS and Beidou timing signals simultaneously, and select the optimal signal as its own clock source.

The schematic diagram of the time synchronization system in the station is shown in Figure 4.

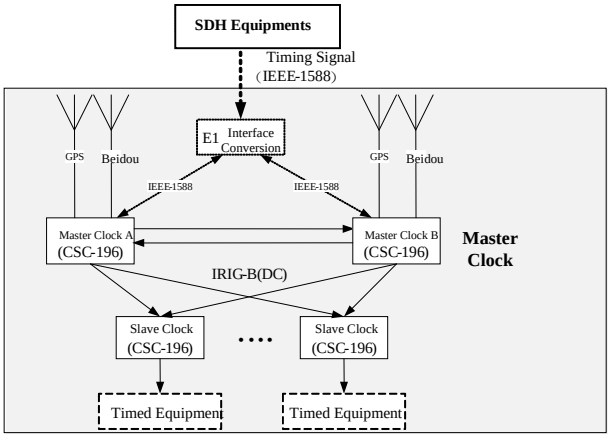

FIGURE IV. STRUCTURE OF INSTATION TIME SYNCHRONIZATION SYSTEM

The clock device in the station can provide IEEE-1588 timing function. By selecting IEEE-1588 timing plug-in, it has two working modes: master and slave. The plug-in is installed in the clock device in the form of an extended card, and the high precision time reference is obtained through the internal bus of the clock device, and the Ethernet output interface of the optical / electric port is provided. The IEEE-1588 plug-in of the clock device uses the hardware platform of "ARM + IEEE-1588 s dedicated PHY", which provides hardware support for the implementation of the IEEE-1588 one-step function. In software, the embedded operating system and Ethernet protocol stack are used to facilitate functional expansion and management.

The overall architecture of the plug-in's hardware and software is shown in Figure 5 below.

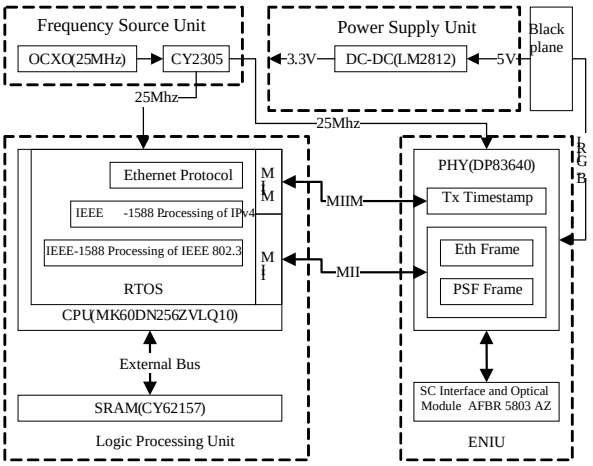

FIGURE V. HARDWARE AND SOFTWARE ARCHITECTURE OF IEEE-1588 FUNCTIONS

B. *Interstation Synchronization Technical Scheme*

After the clock device has IEEE-1588 timing function, it can realize the communication of IEEE-1588 data between stations through E1 protocol converter. The master clock of the station can realize the time synchronization of IEEE-1588 between the Master Slave and the Slave. The structure schematic diagram is shown in Figure 6.

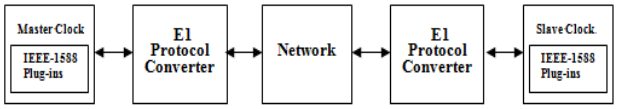

FIGURE VI. APPLICATION OF IEEE-1588 TIMING DEVICE IN SDH NETWORK

Due to the existence of delay jitter and path switching in the network, it is necessary to deal with the calculation of link delay and the calculation of time error when IEEE-1588 is used on the network. That is, targeted processing needs to be done in software.

IV. RESEARCH ON KEY TECHNOLOGY

A. *Study on Time Scale Transfer Technology*

In the V2 version of the IEEE-1588, one-step and two-step methods are defined for the transmission mode of timing mark. Compared with two-step method, one-step method has many advantages, such as saving communication bandwidth effectively and reducing communication delay jitter. However, in the current application of smart substation, the application of IEEE-1588 is mainly based on the two-step method due to limitations of hardware devices. [7] Therefore, in this scheme, the one-step application of IEEE-1588 is studied emphatically.

Currently, when implementing insertion of timing mark using IEEE-1588 one-step method, there are usually two options in hardware design: one is to use the FPGA chip, one is to use the FPGA chip, and implement an Ethernet MAC

function that supports the time stamp insertion function in the FPGA. [8] The second is to use a special chip that can provide the time stamp insertion function, such as the IEEE-1588 dedicated Ethernet PHY chip. In this scheme, because of the small number of IEEE-1588 interfaces in the single board, considering the cost of FPGA chips and the complexity of the development of firmware in FPGA, a special Ethernet PHY chip using IEEE-1588 is selected in the project. This chip supports the V1 and V2 version of IEEE-1588, provides support for one-step method, and provides a variety of clock adjustment interfaces and methods.

The logic processing unit of the IEEE-1588 timing device hardware is based on the low power CPU of a Freescale Kinetis K60 series, which is the core of the entire hardware platform. It is responsible for the processing of the input signal of the backboard, the management of the peripherals, the logic processing of the IEEE-1588 protocol stack, the implementation of the filtering and punctuality algorithm, and the control function of output signal. The hardware logic diagram of the device is shown in Figure 7.

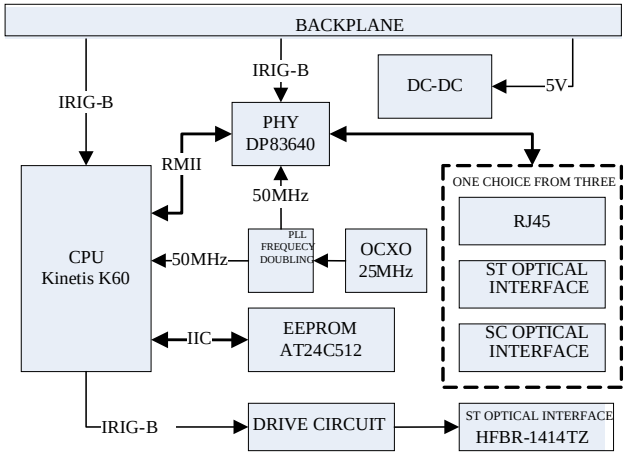

FIGURE VII. HARDWARE LOGIC DIAGRAM OF IEEE-1588 TIMING DEVICE

B. Study on Protocol Stack Technology

Considering that the device has more working modes and more software functional units, the software of the device uses Ucos-II embedded real-time operating system in order to coordinate and manage the functional units.

The processing flow of the device to Ethernet data (IEEE-1588 protocol) is shown in Figure 8, which is mainly divided into the following parts:

1) Ethernet data classification processing:

The processing of this part corresponds to the sequence number 1 in the diagram. In this process, the CPU queries the receiving descriptor of its internal Ethernet MAC to determine whether the complete message is received, and identifies the type, length, source, and destination MAC address of the message. According to the frame type of the packet and the source MAC address, the packet is classified into an IEEE802.3 packet, an IPv4 packet, or a PSF packet, and the packet is encapsulated into a Ucos-II message mailbox, sending to the sequence number of the graph to be followed up for the 2, 3, and 11 processes.

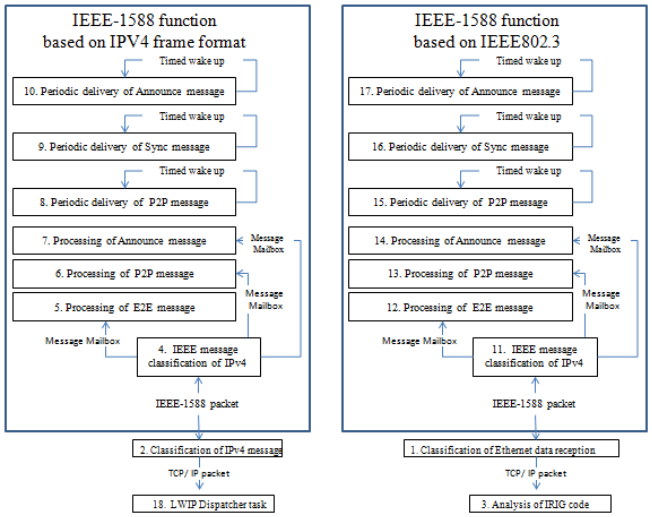

FIGURE VIII. ETHERNET DATA (IEEE-1588) PROCESSING FLOW

2) PSF packet processing (interpretation of IRIG-B code):

The processing of this part corresponds to the sequence number 3 in the diagram. After receiving the message mailbox, the PSF message will be parsed. The time stamp information about IRIG-B code signal changes in PSF message will be extracted, and sent to a FIFO cache with a length of 200. Through the time mark difference value in the neighboring units, the signal pulse width of the input IRIG-B code can be calculated, and corresponding symbols can be obtained to finally parse the UTC time contained in the IRIG-B message.

The UTC time represents the reference time of the IRIG-B message's second punctual time. When the second punctual time edge of IRIG-B code arrives at the master station, the internal time of the master station can be obtained through the time mark in the PSF message. By calculating the difference between the time mark and UTC time, the error between the internal time of the main station and the reference source can be obtained.

3) Classification processing of IEEE-1588 packets in IEEE802.3 frame format

The processing of this part corresponds to the sequence number 11~17 in the figure. The process of 11~14 is mainly the response of the received IEEE-1588 message. The 15-17 process is responsible for the periodic delivery of the IEEE-1588 request message.

4) Classification of IPv4 messages

The processing of this part corresponds to the sequence number 2, 4~10 and 18 in the diagram. In process 2, CPU needs to identify the IEEE-1588 message that is encapsulated in the IPv4 frame format in the UDP message, Then CPU transfers it to process 4 in the form of a message mailbox, and the rest of the message to the number 18 process. In process 18,

the IPv4 frame format IEEE-1588 message will be classified again and forwarded to process 5~7 for subsequent processing. In addition, process 8~10 will also send out IPv4 frame format request packets periodically according to the configuration cycle.

The above four parts constitute a complete IEEE-1588 protocol stack. In actual use, it only needs to be cut through the configuration parameters, so that the corresponding process can provide the required function.

C. Study on Time Conversion Technology

Considering the continuity of timeline, IEEE-1588 chooses TAI (World atomic time) as reference time system. This is due to the leap-second phenomenon in UTC time series, which may cause abnormal operation of the system. However, in the current power system time synchronization system, most devices and equipment use UTC time. Therefore, the problem of TAI and UTC (world coordination) transformation needs to be solved, and the essence of the transformation is the processing of the leap second.

In this project, IEEE-1588 timing device use the following scheme to perform the time - element conversion.

(a) The main clock of IEEE-1588 selects TAI as the reference time system, and the Utc Offset in the Announce message is set as the current leap seconds. The current leap seconds can be acquired by satellite signal receiving board.

(b) The IEEE-1588 device operating in the main mode will receive and parse the reference signals of the external input in real time, and extract the related signs and alarm of the leap second, and fill in the latest information each time the Announce message is sent.

(c) The IEEE-1588 device running in slave mode estimates the leap second time by receiving and parsing the Announce message sent by the IEEE-1588 master station, and converts the estimated leap second value into the leap second symbol defined in the IRIG-B code, which is reflected in the IRIG-B code of the device output.

D. Study on Synchronization Error Correction

Compared to the existing network time synchronization system based on the GPS and the Beidou satellite, the system based on the ground communication network is not susceptible to external factors in the reliability, stability and accuracy of the operation. However, some characteristics of SDH network make it difficult to achieve high-precision timing based on the SDH network. In this paper, through the theoretical analysis of the delay jitter, sliding code, path switching and other phenomena of SDH network, the research of the filtering algorithm for network delay jitter, the recognition conditions and processing methods of sliding code and path inversion are focused on.

When IEEE-1588 is used to achieve time synchronization between stations, the data often need to go through multistage SDH equipment, and data transmission delay on the link in large. If it is not calculated and compensated, there will be a large static error between the stations. This paper uses the E2E delay measurement mechanism provided in IEEE-1588, It is based on the principle of ping-pong timing to calculate the link delay through the Sync message sent by the IEEE-1588 master station, the delay request message sent by the slave station, and the delay response message of the master station.

Considering the physical characteristics of the SDH device, the link delay has a certain amplitude jitter. Therefore, it is necessary to filter the delay jitter when calculating link delay. The filtering algorithm adopted in this paper is based on the first order digital low-pass filtering algorithm, combined with common digital filtering algorithms such as speed limiting filtering and limiting filtering. The formula of the first order digital low pass filter is as follows:

$$Y_n = a \times X_n + (1-a) \times X_{n-1} \tag{5}$$

Where, a is the filter coefficient, whose value is greater than 0 and less than 1; Xn is the current sampling value; Xn-1 is the last sampling value; Yn is the output value after filtering.

On the basis of the first-order digital filtering, when calculating the SDH network link delay, the device periodically puts each calculated delay value into the sample pair, calculate the mean, variance and other statistics of sample pairs, and then carry out the speed limiting filtering and limiting filter processing based on these statistics. Samples with large variance should be discarded directly. For amplitude limiting filtering, we need to set an amplitude threshold and eliminate the samples that exceed the threshold value, and then use the rest to calculate the subsequent link delay. In addition, it should be noted that when the number of sample points removed is large, other criteria should be combined to analyze whether SDH has slippage or path switching. For speed limiting filtering, it is necessary to calculate the change rate between adjacent sample points on the basis of limiting filter. Only when the change rate between all the sample points and the variance of the sample are within threshold range, can the time delay value of this calculation be judged effectively, and used for subsequent time error calculation.

In addition, it should be noted that when the SDH has slip codes and path switching, the mean of the link delays in two adjacent periods is greatly deviated. Therefore, the output needs to be compensated and adjusted accordingly. Each time the timing device of the master and slave station completed the interaction of messages, the time error is further calculated on the basis of the network delay, and then time adjustment is made.

Although the timing device does the processing of buffeting and filtering in the time delay calculation, but it can not completely filter all the interference because the jitter process is random. If using the calculated error without processing and compensated directly, it may lead to a wide range of jitter in time, which may even form positive feedback when it is serious. To solve this problem, the classical PID algorithm in the control system is used when the timing device adjusts the error.

Here, the incremental digital PID algorithm is used. The formula is as follows:

$$\Delta u(k) = K_p \times [e(k) - e(k-1)] + K_i \times e(k) + K_d \times [e(k) - 2e(k-1) + e(k-2)] \quad (6)$$

In the formula, Kp: Proportional adjustment coefficient; Ki: Integral adjustment coefficient; Kd: Derivative adjustment coefficient; e(k): The input value of the kth time; △u(k): Adjustment increment.

When PID arithmetic is used to adjust, the adjustment coefficient is segmented. Different PID adjustment coefficients are used for different magnitudes of errors. In order to ensure good dynamic response characteristics as well as static characteristics, and avoid large overshoot during the adjustment process. For the tuning of PID parameters, the experience trial method is used here.

E. Study on Undisturbed Switching Technology of Multi - clock Source

The undisturbed switching technology of multi - clock source is the core of time synchronization system. In this system, the undisturbed switching function of the multi clock source not only involves the switching of the 3 clock sources of the GPS, the Beidou and the ground wired datum, but also involves the taming of the atomic clocks under the multi reference source, as well as the implementation of the corresponding punctuality algorithm. Therefore, it is necessary to focus on the research of the switching technology.

In the scheme, the handling of the undisturbed switching of multiple clock sources is completed by the main signal receiving board of the CSC-196 device to realize the bumpless switching of Beidou, GPS, and ground reference signals. The undisturbed processing here also covers the punctuality processing of the atomic clock. At the same time, in order to realize the undisturbed switching of the multi clock source, the state of the reference sources should be monitored in real time. The reference source with the best working condition is selected as a reference clock, and the time synchronization signal is output based on this. When the reference clock source is stable, the atomic clock should be tamed so that high-precision punctuality can be achieved when the reference clock source fails.

In order to achieve the above requirements, multi time source information modeling, noise reduction, fusion, fault tolerance and other technologies are used in the process of multi time source non disturbance switching.

1) Noise reduction

Due to limitations in the manufacturing technology and radio signal systems, there are certain timing errors in the crystal oscillator and radio time system, which can be divided into two major categories: random noise and random drift error. The effective processing of the error can not only improve the time accuracy of the combined timing system, but also guarantee the short-term prediction accuracy of the combined timing filter when the satellite timing signal is lost.

For the random noise, a common wavelet threshold denoising method is used to improve the signal-to-noise ratio of the time source signal. The wavelet transform uses Haar mode, and the specific threshold is as follows, and K is an adjustment factor.

$$w_{new} = \begin{cases} sign(w)(|w| - \frac{T}{1+\ln(k\frac{w}{T})^2}), |w| \geq T \\ 0, |w| < T \end{cases} \quad (7)$$

The random drift error can be modeled as the FAR model, and the real-time estimation is made by combining the timing filter. Finally, the output accuracy of time source is improved, and its error model is estimated and corrected in real time.

2) Fusion and fault tolerance

The multi-time source information fusion structure uses the federated structure, which can guarantee the real-time performance of the timing system, and can also make the combination of timing system with better fault tolerance. In the combined filter structure, each sub-filter is relatively independent, especially without resetting structure, and the information distribution of each sub-filter is carried out in local filters in a certain proportion. The main filter has no information allocation, its output is only determined by the time update. The main filter only integrates the estimation information of the local filters, and does not reset the local filter information. Therefore, the local filters work independently and have a strong fault tolerance ability. The only disadvantage is that the precision is slightly lower than the fusion reset structure, but the system reliability and fault tolerance are improved. This scheme is considered to be a fault-tolerant combined filter structure. For the combined timing system, the fusion problem is a nonlinear non-gaussian problem. The positioning algorithm based on EKF (extended Calman filter) can be used to solve the nonlinear problem of the system, thus further improving the timing accuracy of the timing system.

3) Modeling

To solve the dynamic change of each time source error model in the process of system operation, the adaptive interactive multi model method is introduced to carry out fusion filtering to realize the dynamic switching of various time source models. The adaptive interactive multi-model consists of a parallel filter bank and likelihood test algorithm: Firstly, establish the model of the subsystem in normally. operation and typical fault, and each model for a particle filter unit. Then calculate the likelihood function of each filter. By comparing each likelihood function online, the most likely failure model can be determined. For the error model of each time source, a group of particles is randomly selected according to the prior probability density. After input interaction and particle filtering, the particles are resampling, and then the output interaction is conducted. Such continuous recursive propagation updates these particles to complete the estimation of state variables.

In order to give full play to the performance advantages of the two levels feedback structure of the federated filter, the

global intelligent fusion based on fault tolerance judgment can be carried out according to the fault-tolerance performance evaluation results of each subsystem, thereby effectively improving the accuracy, fault tolerance and adaptability of the combined timing system.

F. Study on Taming Technology of Atomic Clock

Atomic clocks can be used to achieve the function of high precision punctuality, but it must be tamed with Beidou and GPS datum before use. The essence of taming is the measurement and compensation of the atomic frequency standard of its output. There are two key indicators to be focused on:

(a) The accuracy and stability of 1PPS output by Beidou and GPS are usually expressed as the normal distribution variance of output 2PPS's time value, generally between 15ns-100ns.

(b) It is necessary to pay attention to the frequency variation characteristics, that is, the frequency changes may occur during the time keeping (missing frequency standard) process.

Usually punctuality can be expressed as:

$$\Delta T = T_0 + \int_0^T \Delta f dt \tag{8}$$

In the above formula, T0 is the initial phase difference and T is the punctual time. △f is the characteristic function of frequency variation, which usually contains the change characteristics of frequency relative to time, temperature, acceleration, radiation field and noise. The characteristic function of the frequency variation is nonlinear, which is related to its aging rate. Its characteristics can be approximated by the following formula:

$$f(t) = A \cdot \ln(B \cdot t + 1) + C \tag{9}$$

In the above formulas, f represents frequency, t indicates time. A, B and C are aging coefficients, and they are different for each atomic clock, so a fixed coefficient cannot be used. To obtain the specific coefficients of A, B and C, it is necessary to make regression analysis on the characteristics of the atomic clock. Since it is difficult to do logarithmic regression directly, the logarithmic regression is converted into linear regression, and the functions of linear regression are as follows:

$$f(t) = A \cdot \ln B + C + A \cdot \ln t \tag{10}$$

After linear regression, the values of A, B, and C can be deduced by means of least-squares method, and it can be used to compensate for aging rate in time keeping.

V. CONCLUSION

In view of the lack of wide-area time synchronization system in power system and the reliability problem of satellite-based time synchronization, this paper proposes to use GPS and BeiDou to build the main and standby time synchronization system in the station. Through the analysis and comparison of different timing methods, the IEEE-1588 protocol has advantages in balancing requirements. Therefore, the IEEE-1588 protocol is used to achieve time synchronization between stations. At the same time, the key technologies are studied while putting forward the technical plan, so that GPS, Beidou and network will form a three redundant time synchronization system. The new time synchronization system can not only overcome the reliability problem of satellite timing source, but also meet the wide area time synchronization requirements of the wide-area stability control system.

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