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A Clock Synchronization Method for Multi Platform Combined Electric Drive Vehicle Real Time Simulation System

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Abstract: In order to realize the clock synchronization function of dSPACE real-time simulation platform, RT-LAB simulation platform, Vortex real-time dynamic simulation system and hardware controller, etc, a hybrid clock synchronization method is proposed in this paper. The master clock server output includes IEEE1588-2008 network clock synchronization signal and second pulse signal. Based on IEEE1588 network clock synchronization signal, the clock synchronization between the master clock and the Vortex simulation platform and the relay board is realized. And the clock synchronization between the master clock and the RT-LAB simulation platform is also realized based on the second pulse signal. In the mean time, the clock synchronization between dSPACE simulation platform and physical controller is realized by FPGA relay board.

1. Introduction

Electric drive is the development direction of armored vehicle transmission system, and also the foundation of all electric combat vehicles in the future. Based on the hardware in the loop simulation technology, the high reliability real-time software / hardware environment (such as dSPACE, RTLAB, etc.) can be used as the technical support, which can meet the high efficiency, precision and rapid design requirements of the electric drive vehicle control system. Improving the efficiency of design and development has become an indispensable research means in the development of control system. The simulation of the electric transmission system of armored vehicles involves mechanical, electrical, control, dynamics and other fields, so a variety of professional software and hardware platforms are needed to carry out joint simulation. In view of the structural features of the electric transmission system of armored vehicles and the functional characteristics of the simulation software in the related fields, the dSPACE real-time simulation platform, the RT-LAB real-time simulation platform and the Vortex workstation can be used to realize the joint simulation of the vehicle integrated control, electric and vehicle dynamics. And the characteristics of the electric drive control strategy and vehicle power are also verified by simulation.

Clock synchronization is the basis of time consistency of each simulation node, and is also an important guarantee for realizing the real-time performance of the system. To verify the credibility of the real-time simulation system, the real-time performance of the real-time simulation system should be analyzed and verified first, and the main factors affecting the real-time performance of the distributed real-time simulation system are emphatically analyzed. According to the clock synchronization problem of multiple single chip computers, Ref. [1] proposed two solutions: the clock synchronization scheme of external clock tree, which uses the same external crystal oscillator to drive all chips simultaneously; The Ref. [2] points out that for the server equipment with network connection function, the mature high precision network clock synchronization protocol, such as the IEEE1588 protocol and the White Rabbit protocol, can realize the high precision clock synchronization of the multi device. However, there is no information about clock synchronization

technology such as dSPACE real-time simulation platform, RT-LAB real-time simulation platform and Vortex workstation.

2. General Scheme of Clock Synchronization

In this paper, a hybrid absolute clock synchronization scheme based on IEEE1588 network clock synchronization technology, second pulse clock synchronization technology and hardware pulse clock trigger technology is proposed by analyzing the existing conditions and combining the characteristics of the existing domestic technology manufacturers, as shown in Figure 1.

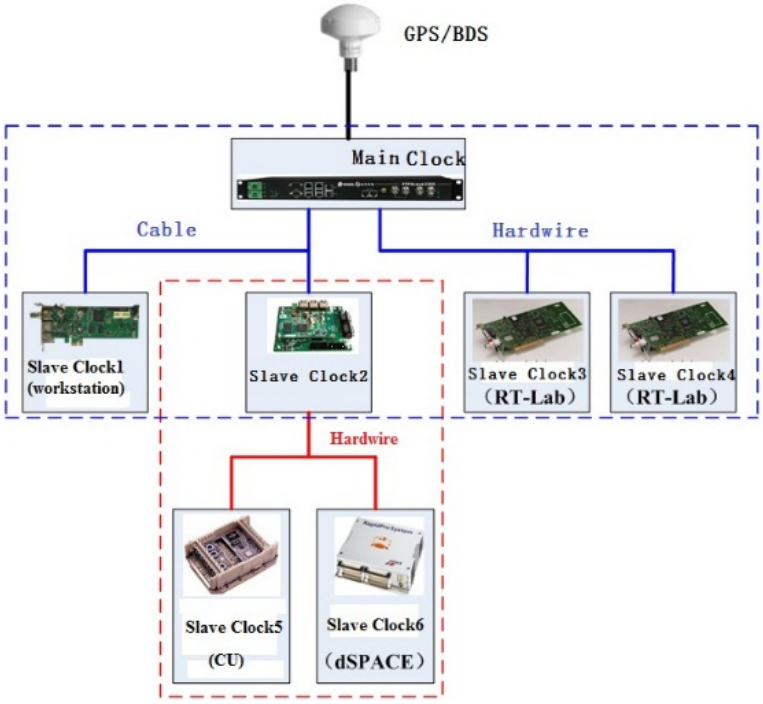


Fig.1 General scheme of clock synchronization

The main clock is the time server of the KW-2200 type, which receives the GPS/ BDS clock signal and establishes the time signal consistent with the natural clock in combination with its own rubidium clock. Slave clock 1 node is a workstation based on Windows operating system； Slave clock 3 and slave clock 4 are RT-LAB simulation nodes. These two kinds of devices all have special clock synchronization device support. Slave clock 5 and slave clock 6 are respectively the integrated controller node and the dSPACE simulation device node. The peripherals are powerful. Therefore, the external interrupt triggering mode can be used to drive the simulation process by using the pulse signals generated by the external clock signal. As an intermediate node, the function of slave clock 2 is to generate clock pulses based on the synchronization with the master clock as a clock signal of slave clock 5 and 6. Specifically, the slave clock 1, slave clock 2 and main clock are connected by a network line, and the clock synchronization is carried out based on the IEEE1588 network clock synchronization method; The slave clock 3, slave clock 4 and the main clock are connected by a hardwire. And the master clock provides 1PPS signals for two slave clock boards to achieve clock synchronization between the three. The slave clock 2 is connected to the slave clock 5 and the salve clock 6 by a hardwire connection, and a clock signal is provided from the slave clock 2.

3. Sub System Function Implementation

According to figure 1, the clock synchronization system mainly includes three parts: the clock synchronization based on the IEEE1588 network clock synchronization signal and the Vortex simulation platform and the relay board, the clock synchronization of the main clock based on the

second pulse signal and the RT-LAB simulation platform, and the clock synchronization of the relay board based on FPGA, the dSPACE simulation platform and the physical controller.

3.1 Clock Synchronization Based on IEEE1588 Network.

The network clock synchronization system based on IEEE1588 includes 4 parts: GPS/ BDS signal receiver, 1 main clock server and 2 slave clock boards. The master clock server is connected to the slave clock with shielded wires by a high-performance router, as shown in Figure 2.

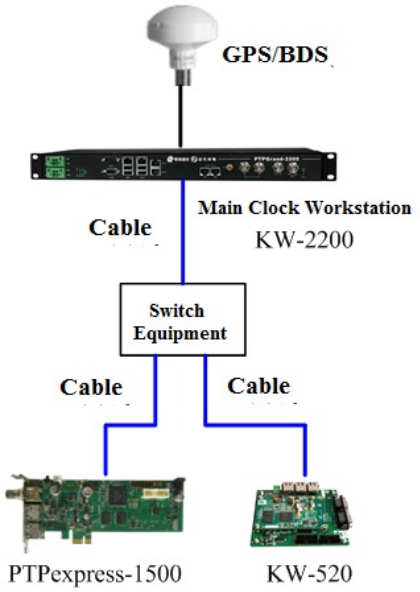


Fig. 2 IEEE1588 network clock synchronization system

The specific working process of the IEEE1588 network clock synchronization system is as follows: firstly, the main clock server receives the time signal on the satellite through the GPS/ BDS signal receiver and gets the absolute time signal after processing. Secondly, the master clock communicates with two slave clock boards based on the IEEE1588 network clock synchronization protocol, and realizes the synchronization of two slave clock boards and the main clock server. Then, when the Vortex workstation simulates, through the corresponding API function, the synchronization time information is read in the high precision time service board based on PTPExpress-1500, and the simulation program is run based on this time information. At the same time, the KW-520 based on the synchronization time information sends out the clock pulse signal of the corresponding frequency according to the system requirements, which is used as the clock signal of the lower level simulation node.

3.2 Clock Synchronization Based on Second Pulse.

As the PCI-SYNCCLOCK32-UNIV clock synchronization board supported by the RT-LAB simulation system only supports IRIG A&B, NASA36 and second pulse input, and the master clock server KW-2200 has a second pulse signal output, therefore, a new clock synchronization network can be formed based on the second pulse signal, as shown in Figure 3.

The principle is as follows: the local clock crystal vibration is counted in the second pulse time of a specific number. The actual frequency of the local clock can be obtained by the count value, and then the frequency error can also be obtained. Eventually the frequency correction based on this error value is carried out.

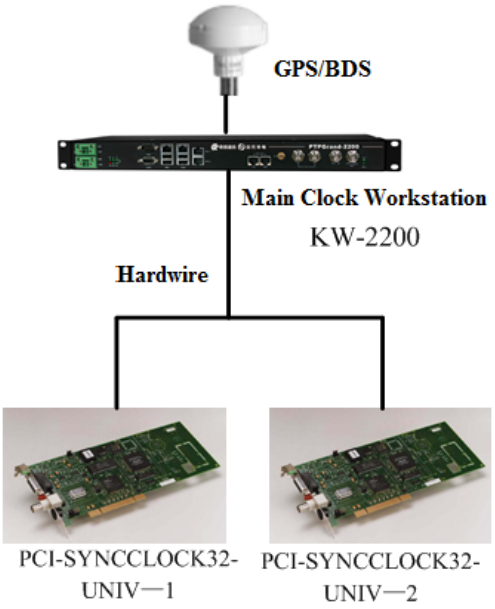


Fig. 3 Clock synchronization system based on second pulse signal

3.3 Clock Synchronization Based on FPGA.

In order to synchronize the time of the real vehicle integrated controller, the dSPACE simulation platform and the master clock server, the KW-520 clock synchronization board based on FPGA is needed as an intermediate node to connect the two layers of synchronization network, as shown in Figure 4.

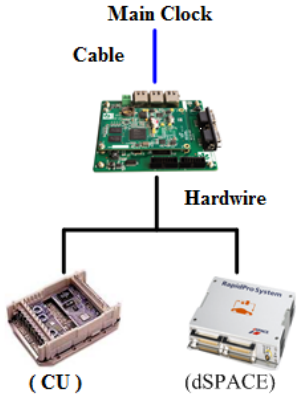


Fig.4 Hardware clock synchronization architecture based on FPGA

In the practical application of the system, the frequency pulse signal output function of KW-520 is mainly used. KW-520 adjusts its own clock by synchronizing the clock with the main clock KW-2200 through the IEEE1588 network clock synchronization. According to the demand, the output square wave pulse signal is used as the clock signal to drive the lower level simulation nodes. The maximum pulse frequency is 10MHz, and the minimum pulse period is 0.1μs. Therefore, the minimum simulation step of the lower level simulation node can reach 0.1μs. The KW-520 output pulse signal is mainly used to drive the real vehicle controller and dSPACE simulation system. For the real vehicle controller, the external interrupt triggering mode can be used, and the interrupt signal is generated by the rising edge of the external pulse, which triggers the operation of the interrupt subroutine. The simulation step can not only realize the frequency doubling of the minimum simulation step (0.1μs) by the method of accumulating the counter, but also can be changed by setting the pulse frequency of the KW-520 directly. The clock synchronization principle of dSPACE simulation system is similar.

4. Real-time Synchronization Performance Test

After the clock synchronization system network is completed, the clock synchronization performance of each simulation node needs to be tested to determine whether it meets the simulation design requirements. However, because the system contains many types of node devices, the performance of devices, the type of interface and the type of clock synchronization signal are quite different. During the simulation, it is difficult to collect the real clock signals of the simulation nodes at the same time, so it is very difficult to test directly.

Through the analysis of the clock synchronization equipment of each node, it is known that the current clock synchronization device can realize the output function of the second pulse, and the output signal is all the signal after the synchronization of various internal clocks, and the synchronization performance of the second pulse signal also represents the clock synchronization effect of the device itself. For the hardware clock synchronization part based on FPGA, the second pulse signal of the intermediate node KW-520 output is connected by the two sub simulation nodes of the hardwire and the lower layer. The second pulse signal is directly driven by the clock signal to drive the simulation program. The intermediate process is very short and can be ignored, therefore, the synchronization effect of the second pulse signal output by KW-520 can represent the clock synchronization effect of its lower level nodes.

In conclusion, the clock synchronization performance of the whole distributed clock synchronization device can be obtained by measuring the second pulse synchronism of the main clock server and the four clock synchronization devices. The system test structure is shown in Figure 5.

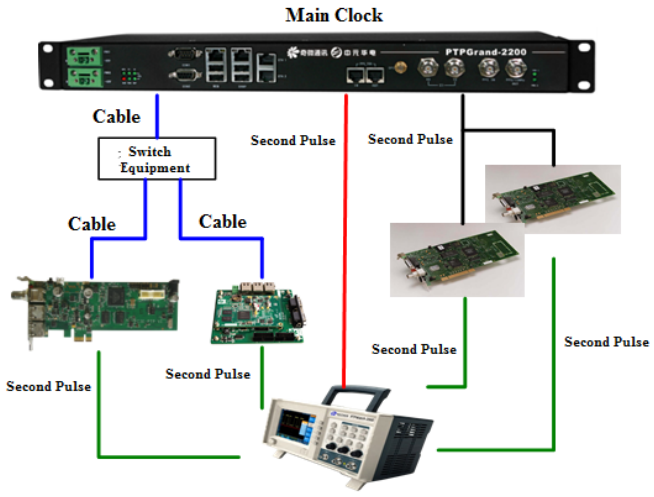
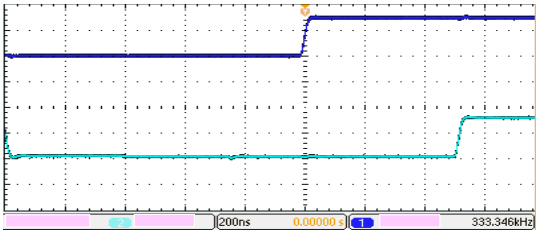


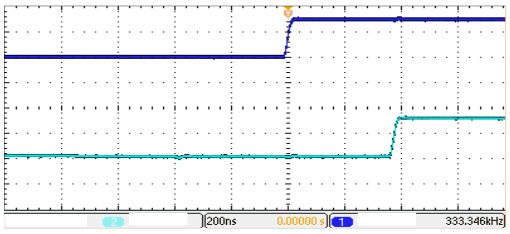
Fig.5 Test block diagram of clock synchronization system

When the system runs, the second pulse signals output by PTPExpress-1500 high precision timing board, KW-520 clock synchronization board and two PCI-SYNCCLOCK32-UNIV clock synchronization boards are compared with the second pulse signals from the main clock output, and the high performance oscilloscope is used to observe the signals. The recorded waveforms are shown in Figure 6, respectively.

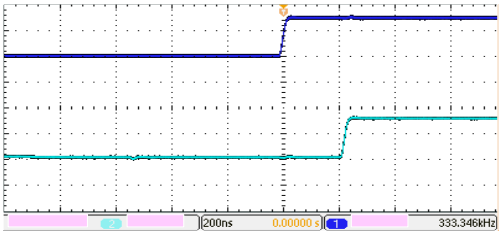
As seen from the Fig.6, the second pulse error of the PTPExpress-1500 high precision timing board and the master clock server is about 0.5μs, and the second pulse error of the KW-520 clock synchronization board and the master clock server is about 0.35μs, and the second pulse error of the two PCI-SYNCCLOCK32-UNIV clock synchronization boards and the main clock server is 0.21μs and 0.2μs respectively. The minimum simulation step of the real time simulation system of the wheel motor driven vehicle is 20μs. The above stated errors fully satisfy the clock synchronization performance requirements of the real-time simulation system.



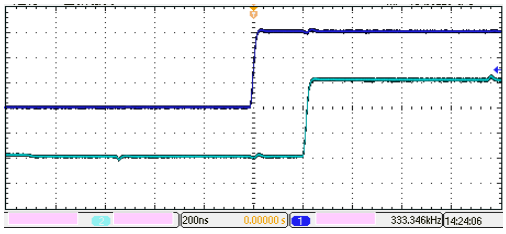
(a) The error of PTPExpress-1500 high precision time board second pulse



(b) the error of KW-520 clock synchronization board second pulse



(c) The error of 1# PCI-SYNCCLOCK32-UNIV synchronous board second pulse



(d) The error of 2# PCI-SYNCCLOCK32-UNIV synchronous board second pulse

Fig 6. The test results of the clock synchronization performance

5. Conclusion

In this paper, a hybrid clock synchronization system of distributed real-time simulation system is designed to synchronize the Vortex simulator, dSPACE simulator, RT-LAB simulator, real vehicle controller and master clock server. The test system is designed, and the clock synchronization performance of the system is tested by the output of each node. The test results show that the clock synchronization system can improve the time consistency of the simulation nodes and meet the real-time simulation requirements of the system, which is of great significance for improving the system simulation accuracy and the reliability of the simulation.

References

[1] Sun yongcheng, sun ling, zhou xianzhong, et al, Real-time verification of distributed real-time simulation system, Journal of system simulation. 17 (2005)1553-1555.

[2] Wu baoxin, Guo yonghong, Cao Yi, et al, Development practice of automobile FlexRay bus system, Electronic Industry press, Beijing, 2012.

[3] Guruswamy, A. Blum, R S, Kishore S, et al, Minimax Optimum Estimators for Phase Synchronization in IEEE 1588, IEEE Transactions on Communications. 63(2015)3350-3362.

[4] Liao Ying, Liang Jiahong, Yao Xinyu, Real-time simulation theory and support technology, National University of defense and Technology press, Changsha, 2002.

[5] Yao Xinyu, Huang Kedi, Real-time analysis of semi-physical simulation system, Computer simulation. 16(1999)51-54.

[6] Pan Yulin, Yao Xinyu, Chen Yong, et al, High precision time management of parallel distributed real-time simulation , Journal of system simulation. 21(2009)154-156.

[7] Li Shaoyan, Hui Tianshu, Chen Zongji, Implementation technology research of the LAN-based distributed real-time simulation, Journal of system simulation. 16(2004)1489-1493.

[8] Li Shaoyan, Hui Tianshu, Chen Zongji, Scheduling strategy research in LAN-based distributed real-time simulation, Journal of system simulation. 15(2003)1024-1029.