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# Improved Electrical Performance for Multilayer $MoS_2$ Transistors by Using a Fully Encapsulated $Al_2O_3$ Dielectric Layer

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**Keywords:** multilayer $MoS_2$, fully encapsulated $Al_2O_3$, transistor, field effect mobility

**Abstract.** A fully encapsulated $Al_2O_3$ dielectric is developed to improve device performance in multilayer $MoS_2$ transistors. Compared with bottom gated $MoS_2$ field effect transistors, top gated transistor with top $Al_2O_3$ dielectric layer and bottom $Al_2O_3$ passivation layer shows great electrical property improvement with an on-off current ratio of $2\times10^5$, a threshold voltage of 0.5 V, a subthreshold swing of 120 mV/dec and a high field effect mobility of 79 $cm^2\ V^{-1}\ s^{-1}$, which are ascribed to optimized device structure as top gate/$Al_2O_3$/$MoS_2$/$Al_2O_3$/$SiO_2$/Si. Low threshold voltage and high field effect mobility are propitious to low power consumption solid-state electrons.

## Introduction

Molybdenum disulfide ($MoS_2$) is one of the most promising 2D materials for electronic switching, due to its relatively high intrinsic electron mobility and thickness dependent band gap ranging from 1.2 to 1.8 eV[1]. $MoS_2$ based field-effect transistors (FETs) have received tremendous attention because they provides a way to miniaturize the device into an atomic scale to reduce the dimension and the power consumption[2]. Radisavljevic et al. fabricated single layer $MoS_2$ FETs, which exhibited high current on-off ratio with $10^8$ and low subthreshold gate voltage swing with 70 mV/dec[3]. Xie et al. prepared monolayer $MoS_2$ transistors, when channel length is above 9 nm, devices are free of short channel effects with current on-off ratio above $4.5\times10^7$, and field effect mobility larger than 30 $cm^2\ V^{-1}\ s^{-1}$[4]. However, the complicated process of fabricating single layer $MoS_2$ may significantly limit its compatibility with commercial fabrication. Multilayer $MoS_2$ (ML $MoS_2$) FETs show higher mobility and larger drive current than those of single layer $MoS_2$ FETs, owing to the reduced interaction distance between various interfacial scattering sources and the carriers within the channel, and multiple conducting channels created by field effect[5]. Thus, ML $MoS_2$ can be more attractive for FET application than single layer $MoS_2$. With the successful application of high-κ gate dielectrics in silicon CMOS processing, which are also considered extensively for $MoS_2$ transistors, owing to the reduction of the gate leakage and the enhancement of the gate capacitance density. Further more, high-κ gate dielectrics can also improve device performance by introducing higher carrier density and dielectric screening effects resulting from thin insulators[6]. Hitherto, ML $MoS_2$ transistors with high-κ gate dielectrics are illustrated by many researchers, and these device parameters which can be found for top or bottom gated transistors in literatures are summarized and listed in Table I.

High-κ dielectric caped on multilayer $MoS_2$ surface for bottom gate (BG) FETs[8] and ML $MoS_2$ channel with backside high-κ dielectric for top gate (TG) FETs [18]can increase field effect mobility and improve subthreshold swing. $Al_2O_3$ grown by atomic layer deposition (ALD) has been widely utilized in $MoS_2$ FETs, as can be seen from Table I. In this paper, we proposed a novel dielectric construction, fully encapsulated $Al_2O_3$ was applied to prepare high performance ML $MoS_2$ FETs. By using 9 nm fully encapsulated $Al_2O_3$ as gate insulator and channel back surface passivation layer, a low threshold voltage of 0.5 V and a small forward/backward threshold voltage shift of 0.3 V have been achieved for TG ML $MoS_2$ FET, with an on-off ratio of $2\times10^5$, a subthreshold swing of 120 mV/dec, and a high mobility of 79 $cm^2\ V^{-1}s^{-1}$. By combining ML $MoS_2$ and fully encapsulated $Al_2O_3$,

the dimension of the transistors can be further decreased with low power and high performance to realized the route of portable electronics.

Table 1. Device parameters summarized from literature.

| Ref. | $t_{MoS2}$/ [nm] | dielectrics/$t_{ox}$[nm] | Construction | $L_{gate}$/ [μm] | Mobility/ [$cm^2V^{-1}s^{-1}$] | On-off ratio | $V_{th}$/ [V] | ss/ [mV/dec] |
|---|---|---|---|---|---|---|---|---|
| 7 | 3 | $Al_2O_3$/72 | $MoS_2/Al_2O_3$/Si BG | 2 | 25 | $10^3$ | | … |
| 8 | 9.8 | $Al_2O_3$/45 | $MoS_2/Al_2O_3$/Si BG | 4.6 | 20.5 | $10^7$ | | 233 |
| 8 | 9.8 | $Al_2O_3$/45 | $HfO_2/MoS_2/Al_2O_3$/Si BG | 4.6 | 25.2 | $10^5$ | | 549 |
| 9 | 30 | $Al_2O_3$/50 | $MoS_2/Al_2O_3$/Si BG | 20 | 100 | … | | 69 |
| 10 | 60 | $Al_2O_3$/50 | $MoS_2/Al_2O_3$/Si BG | 35 | 70 | $10^6$ | | … |
| 11 | 5-7 | $HfO_2$/30 | $MoS_2/HfO_2$/Si BG | 1 | 65 | $10^6$ | | 100-110 |
| 12 | 32.5 | HfTiO/39.6 | $MoS_2$/HfTiO/Si BG | 3 | 31.1 | $5\times10^3$ | | 100 |
| 13 | 1.4 | $ZrO_2$/10 | $MoS_2/ZrO_2$/Si BG | 15 | 64.66 | $10^8$ | | 100 |
| 14 | 2L* | $ZrO_2$/5.8 | $MoS_2/ZrO_2$/BG/$SiO_2$/Si | $10^{-3}$ | … | $10^6$ | | 65 |
| 15 | 3L* | $HfO_2$/Al:$HfO_2$(10/10) | $MoS_2$/ $HfO_2$/Ni/ Al:$HfO_2$/Si BG | 3 | … | $10^5$ | | 57 |
| 16 | 4L* | $Al_2O_3$/24 | TG/$Al_2O_3/MoS_2$/sapphire | 2 | 5.9 | $10^4$ | | … |
| 17 | 5 | $HfO_2$/8 | TG/ $HfO_2/MoS_2/SiO_2$/Si | 5.5 | 20 | $10^5$ | | 350 |
| 18 | 4-5 | $HfO_2$/4 | TG/ $HfO_2/MoS_2/SiO_2$/Si | … | 11 | … | | 154 |
| 18 | 4-5 | $HfO_2$/4 | TG/ $HfO_2/MoS_2/Al_2O_3$/Si | … | 33 | $10^6$ | | 69 |
| 19 | 15 | $Al_2O_3$/10 | TG/$Al_2O_3/MoS_2/SiO_2$/Si | 9 | 517 | $10^8$ | | 140 |
| 20 | 3-5L* | $HfO_2$(28)/$Y_2O_3$(3-7) | TG/$HfO_2/Y_2O_3/MoS_2/SiO_2$/Si | 3 | 47.7 | $10^8$ | | 110 |
| 21 | 7 | $Ta_2O_5$/31 | TG/$Ta_2O_5/MoS_2/SiO_2$/Si | 3 | 61.5 | $10^5$ | | 61 |

*L–layer number

## Experimental Details

Before device fabrication, 300 nm $SiO_2$ was thermally grown on highly doped *p*-type Si wafers (resistivity ~ 0.01 Ω • cm) as substrates. An amorphous layer of $Al_2O_3$ was firstly deposited on $SiO_2$/Si substrate by an ALD process using trimethylaluminum(TMA) and $O_2$ as a precursor and a reactant, respectively. The deposition temperature was maintained at 180°C and the gas injection schedule for one cycle of deposition was 0.02/15/0.02/10 seconds for the TMA/$N_2$/$O_2$/$N_2$ gases. The deposition was finished after 100 whole cycles, and the resulted thickness was 9 nm as measured by atomic force microscope. ML $MoS_2$ flakes were then mechanically exfoliated from bulk $MoS_2$ crystals and transferred on the substrate. The typical $MoS_2$ flakes thickness studied in this work was about 10–15 layers (7–10 nm). Source/drain regions (50 μm×100 μm) were defined on top of $MoS_2$ flakes using e-beam lithography (EBL, JEOL 6510 with Nanometer Pattern Generation System), Cr (15 nm) and Au (50 nm) were deposited by electron-beam evaporation at room temperature, followed by a metal liftoff. Subsequently, another layer of $Al_2O_3$ film was deposited on device surface as mentioned above, thus the ML $MoS_2$ was fully encapsulated with $Al_2O_3$ dielectrics, and Si BG transistors were fabricated. TG $MoS_2$ FETs have also been prepared to enable their practical electronic applications in integrated logic circuits, because bottom gate is a common gate, which can not individually control each transistors on wafer. The top gate electrode was defined using second EBL. Ni/Au (15 nm/50 nm) stack was deposited on top $Al_2O_3$, followed by a final metal liftoff. The device was then annealed at 200°C in a vacuum tube furnace for 2 hours to remove resist residue and to decrease contact resistance.

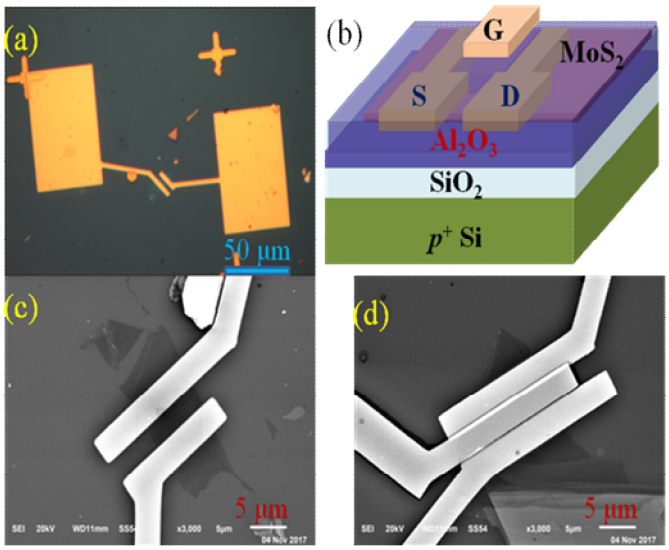


Fig.1 (a) Optical microscope image of the BG ML $MoS_2$ FET, (b)3D-Schematic diagram of a TG ML $MoS_2$ FET. (c) SEM image of the fabricated BG ML $MoS_2$ FET, Source/drain contacts are Cr(15nm)/Au(50nm), (d) SEM image of the fabricated TG ML $MoS_2$ FET, top gate contact is Ni (15nm)/Au(50nm).

The thickness of $MoS_2$ and $Al_2O_3$ are measured using an AFM (SPM-9500J3, Shimadzu, Japan). Scanning electron microscope (SEM) is applied to define channel length and width. Electrical characterizations are carried out with current-voltage measurements (Keithley, Semiconductor Characterization System 4200-SCS). All measurements are taken in dark and electromagnetic shielding. The bottom gate was grounded in all top gate electrical parameter measurements.

## Results and Discussion

Fig. 1(a) illustrates an optical microscope image of the BG ML $MoS_2$ FET. Fig. (b) depicts a 3D-Schematic diagram of the TG ML $MoS_2$ FET. Fig. 1(c) and (d) are SEM images of the fabricated $MoS_2$ FET. Gate length as 3μm is designed on photo mask, the device sizes of most transistors determined by both lithography and the flake shape are about 2 μm and 4-10 μm for the gate length and width, respectively.

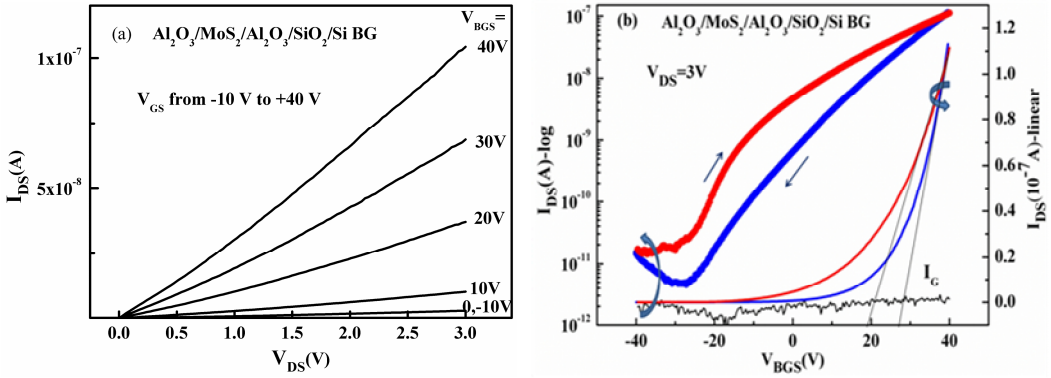


Fig. 2. Operation characteristics of bottom gate ML $MoS_2$ FETs, with W/L = 6/2 μm. (a) Output characteristics. $V_{DS}$ was swept from 0 to + 3 V at each $V_{BGS}$ varing from −10 to +40 V at 10 V step. (b) Transfer characteristics (@$V_{DS}$ = +3 V) and gate leakage current (@$V_{DS}$ = 0 V), $V_{GS}$ was swept from −40 to +40 V.

Fig. 2(a) shows the typical output characteristics of the BG ML $MoS_2$ FETs with fully encapsulated $Al_2O_3$, concretely, fully encapsulated $Al_2O_3$ is applied as $Al_2O_3/SiO_2$ stack bottom gate insulators and

top $Al_2O_3$ passivation layer. An unsaturation behavior of the drain-source current can be observed at high gate bias up to 40V for BG FETs, indicating weak control capability of the gate bias voltage to the $MoS_2$ channel, which can be ascribed to thicker dielectric layer, and intensely pinning of the Fermi level at the $MoS_2/Al_2O_3$ interface.

Transfer characteristics of the BG ML $MoS_2$ FET are depicted in Fig.2(b). The curves clearly display an n-type behavior with on-off ratio as ~ $10^4$ at drain-source voltage $V_{DS}$ @+3 V. The gate-leakage current is lower by half than the off-state current, which indicates that the impact of gate leakage on the electrical characteristics of the BG FETs can be ignored. The threshold voltage ($V_{th}$) extracted from the linear extrapolation method through the maximum slope point of the $I_{DS}$–$V_{BGS}$ curve, is about 19 V, which should be ascribed to the substantial fixed negative charge in the dielectric layer or/and the $MoS_2/Al_2O_3$ interface, probably resulting from the derivation of the impurity charger during the process of $MoS_2$ flakes transferring and adhering. Subthreshold swing (*SS*) is higher than V/dec magnitude, which is owing to enormous density of trapping states at the interfaces. A large positive direction shift of $V_{th}$ drawn from forward/backward transfer curves for the BG FET can be observed, which should be attributed to that the neutral defects capture electron from the channel and become charged, resulting in an increasement of net negative charge density, thus $V_{th}$ become more positive[22]. Obviously, the $V_{th}$ and *SS* for these BG ML $MoS_2$ FETs are not suitable for low power electronics. The field-effect electron mobility was extracted from the liner regime of the transfer curve using the equation $\mu_{FE} = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right) \times \frac{L}{WC_{OX}V_{DS}}$, where $L$ is the channel length, $W$ is the channel width, $C_{ox}$ is the capacitance of the $SiO_2/Al_2O_3$ stack gate dielectric between the channel and the bottom gate per unit area. The calculated $\mu_{FE}$ of BG ML $MoS_2$ FET is 4.3 $cm^2\ V^{-1}\ s^{-1}$, which is lower than those of bottom gate ML $MoS_2$ FETs reported in Ref.7-13 due to small gate capacitance density supplied by thick stack dielectric layers.

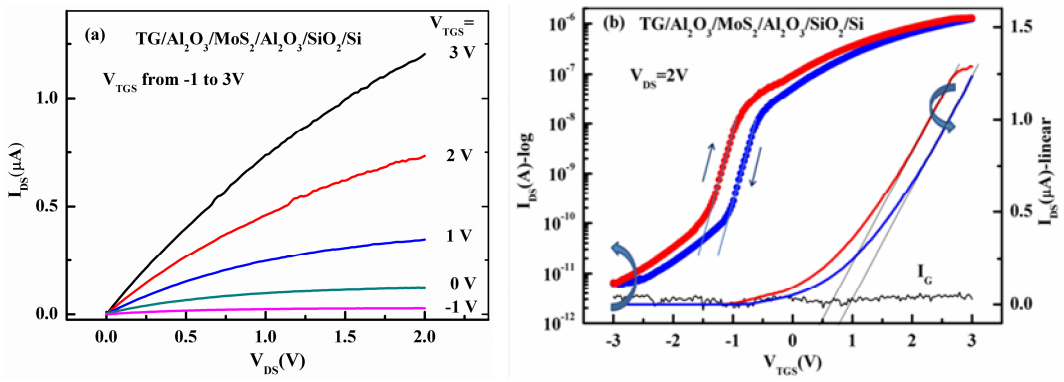


Fig. 3. Operation characteristics of top gate ML $MoS_2$ FETs, with W/L = 6/2 μm. (a) Output characteristics. $V_{DS}$ was swept from 0 to + 2 V at each $V_{TGS}$ varing from −1 to +3 at 1 V step. (b) Transfer characteristics (@$V_{DS}$ = +2 V) and gate leakage current (@$V_{DS}$ = 0 V), $V_{GS}$ was swept from −3 to +3 V.

To further evaluate the properties of the fully encapsulated $Al_2O_3$ for ML $MoS_2$ FETs, top gate transistors were fabricated and measured, because many top gate $MoS_2$ FETs exhibit superior performance than their bottom gate counterparts [6]. Slight current saturation at +2 V drain/source voltage can be seen from Fig.3(a), and 1.2 μA drain current has been achieved, which is one order of magnitude higher than that of BG ML $MoS_2$ FET mentioned above, and this is important for digital circuit application. Large drain current is arised from high gate capacitance density of the thin dielectric, and increased field effect mobility resulting from improved quality of the channel/dielectric interface by ALD process of $Al_2O_3$ grown on $MoS_2$, instead of transferring $MoS_2$ on $Al_2O_3$.

A low $V_{th}$ of ~ 0.5 V can be obtained for TG FET from Fig.3(b), indicating superior control capacity of gate voltage to conduction channel. This threshold voltage is the smallest compared with those which can be found or extracted from literatures listed in Table I. Low $V_{th}$ is essential for low power consumption electron devices, because the real applications as TFTs in OLED displays are operated in "on" state.

The transfer characteristics of the TG $MoS_2$ FET show small shift of $V_{th}$ (~ 0.3 V), which is comparable to commercially available SiO2 (300 nm) [11], indicating the creation of electron trapping states at the channel/gate-dielectric interface during the gate voltage scanning can be neglected. An unchanged *SS* (120 mV/dec) can be also extracted from the transfer characteristics, illustrating a low density of traps at the interface of $MoS_2/Al_2O_3$. An on-off current ratio with $2\times10^5$ can be achieved for TG $MoS_2$ FET, which is higher than that of BG $MoS_2$ FET mentioned above, and at the same level compared with those reported in Ref. 17, 21 for TG $MoS_2$ FETs. The calculated $\mu_{FE}$ of TG ML $MoS_2$ FET is up to 79 $cm^2\ V^{-1}\ s^{-1}$, which is much lower than 517 $cm^2\ V^{-1}\ s^{-1}$ reported in Ref.19, but higher than vast majority data related with both bottom and top gate devices listed in Table I. The increased $\mu_{FE}$ can be explicated as follow. Firstly, carrier scattering is effectively suppressed by superior interface properties between the $MoS_2$ channel and the top $Al_2O_3$ dielectric. Secondly, the top high-κ dielectric changes the dielectric environment and effectively screens Coulomb scattering[2], and the charge traps have been screened by higher carrier density resulting from large gate capacitance coupled [6]. Lastly, backside $Al_2O_3$ layer improves the mobility by passivation effects[18]. These mechanisms enhance the device performance, indicating that a full encapsulated $Al_2O_3$ high-κ dielectric layer is a promising alternative to practical application for top gate multilayer MoS2 FETs.

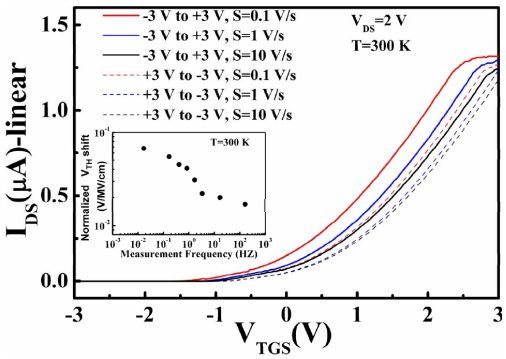


Fig.4 The $I_{DS}$–$V_{TGS}$ characteristics of TG ML $MoS_2$ FET measured using the $V_{TGS}$ bi-directional sweep and different sweep rates. The inset shows the normalized $V_{TH}$ shift versus the measurement frequency.

The threshold stability of a transistor is a key requirement for use in a wide range of application, and the hysteresis is known to be strongly dependent on the sweep rate and the sweep direction [22]. Fig. 4 illustrates the hysteresis of the TG ML $MoS_2$ FET by measuring the transfer characteristics under bi-directional sweep with various sweep rates of 0.1V/s, 1V/s and 10 V/s, respectively. The change of the $V_{TH}$ versus the measurement frequency is presented as inset in Fig. 4, where the $V_{TH}$ is normalized by the oxide field factor [23]. The TG ML $MoS_2$ FET exhibits nearly two order of magnitude improvement of the normalized $V_{TH}$ shift compared to that of the exfoliated bare $MoS_2$ transistor [23], and the comparable $V_{TH}$ shift to the $Al_2O_3$-encapsulated CVD-grown device reported by Illarionov et al. [23]. Small $V_{TH}$ shift indicates the creation of electron trapping states at the channel/gate-dielectric interface during the gate voltage sweeping can be neglected.

## Conclusion

In summary, multilayer $MoS_2$ field effect transistors with fully encapsulated $Al_2O_3$ high-κ dielectric layers as both bottom gate and top gate have been prepared. Enhanced electrical

performance can be demonstrated by top gate devices eventhough without back gate bias, which show desirable electrical characteristics such as a high on-off current ratio, a small shift of threshold voltage, a low subthreshold swing, and a high field effect mobility, compared with bottom gate transistors. The improved device performance for top gate transistors can be attributed to the novel fully encapsulated $Al_2O_3$ architecture. With further optimization of the fully encapsulated $Al_2O_3$ dielectric, the top gate/$Al_2O_3$/$MoS_2$/$Al_2O_3$ integration strategy can be widely applied in low energy consumption electronics.

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