A High Performance ASIC Interface for MEMS Gyroscope

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Abstract. This paper presents the ASIC design and implementation for micro-machined gyroscope, The ASIC interface is including an analog ASIC and a digital ASIC, and can afford driving closed-loop, On-chip reference generation, CIC and IIR filter chain, High performance MEMS gyroscope output detection. The two ASICs are implemented in 0.18μm HVCMOS technology operates with a single 5V supply. The ASIC employ a 4th-order CRFF architecture for achieving high SNR performance. The sampling frequency of the SDM is 2 MHz. And filter chain (including CIC and IIR)with the mechanical sensor element to reject the excessive in-band quantization noise and the resonance signal in the sense of the Gyroscope. The C/V conversion is implemented with continuous capacitance detection , and 4th-order sigma-delta modulator is implemented with switched-capacitor techniques, The gyroscope`s resonance frequency is locked by PLL, and constant drive amplitude in a closed loop system.

Introduction

The market growth of micro-machined（MEMS） gyroscope applications is pushing for developing high performance interface solutions. This paper presents a fully integrated analog and a digital ASIC to interface with MEMS gyroscopes in drive-closed loop and sense-open loop configuration for best performance in harsh environment. Which utilizes the PLL in drive frequency control and PID in drive amplitude control. The *4th-order CRFF architecture low-pass SDM*(sigma-delta-modulator) and filter chain are used in gyroscope sense-loop to achieve high level in gyroscope signal detection.

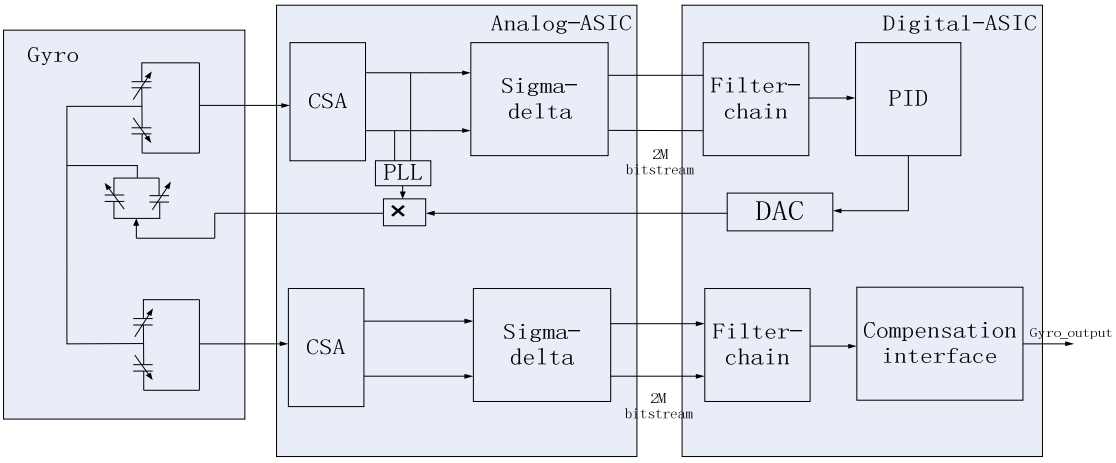

Fig.1 Gyro / ASIC system architecture

Fig.1 shows the block diagram of the ASIC interfaced to a MEMS gyroscope. The system is composed of a gain adjustable low noise capacitive sensing front end, 4th order CRFF sigma-delta modulator [1], 7-step mid-rise quantizer, high precise digital filter chain, polynomial-calculation-unit, are used in capacitive signal digitization. The digital control and compensation processing, are forming the drive and sense loops control and demodulating. The ASIC also have a standard SPI

interface with containing even parity check and a (1k×16bit) Nvram. And is powered from a single 5V supply. The chip employs a low-noise band-gap reference (BGR) core that generates a 1.65V and 0.9V reference voltage required by power-management regulators and other bias cores.(such as be used in modulator reference).

The gyroscope Drive loop

The drive loop, shown in Fig.2, is including two operation modes, one is startup-mode: ensure reliable startup of the MEMS oscillation; the other is normal-mode: maintain stable oscillation of the MEMS gyroscope. Owing to Without MEMS oscillation there is no signal for the PLL to lock to, the multiple sweep cycles are necessary. Modified additional current source for sweeping the MEMS oscillation. Especially is for low amplitudes the zero crossing signal may be disturbed by noise, PLL with PFD(phase frequency detector) cannot lock to such signal (frequency information wrong),In order to obtain the reliable drive oscillation, the PFD in PLL is modified. As the phase signal of oscillation of the MEMS Gyroscope is availability, Startup-Mode is over, the Normal-Mode start to work. Normal-Mode incorporates the phase shift required to achieve the oscillation condition: an PID gain control loop to control the amplitude of oscillation of the mechanical element. A 4th-order low pass modulator, composed of two resonators with feed forward coefficients, converts the drive loop C/V output into three bit reading of the gyro drive oscillation signal. The condition of phase between force and drive amplitude is n*360°and the amplitude continue to be constant value.

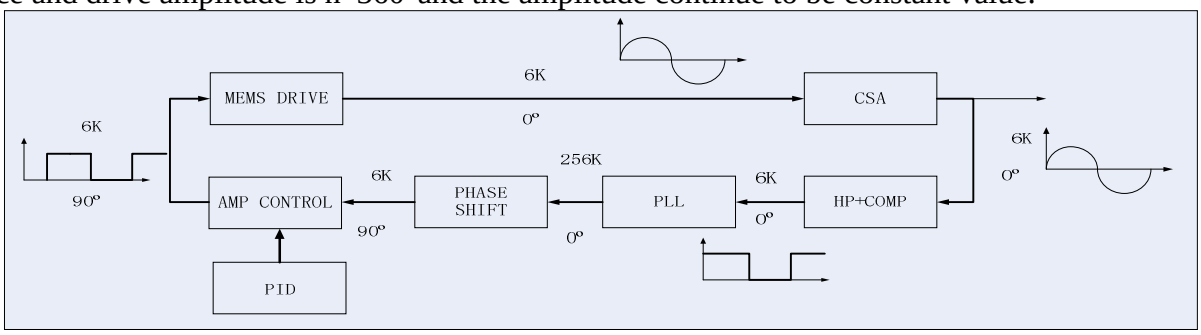

Fig.2 Gyro drive frequency and amplitude control architecture

Capacitance to Voltage Front End (C/V) Interface

The capacitance-to-voltage front end (C/V) interface, shown in Fig.3, is implemented by using a continuous time capacitance to voltage converter for gyroscope drive and sense. The low noise differential amplifier is used for fulfilling the fully differential design can reject common mode noise better. The feedback resistor realized as PMOS device. C/V converter with gain depends on Cint and the constant voltage difference between mass and VCM is Vb, VCM=1.65v means that if the mass is 5v, the Vb is 3.35V. The output signal Vo is simplified formula (1) .part 1 in Fig.3 is also PMOS device as the function is a switch, the different C/V converter gain by use of switch on or off. The design of adjustable gain is for maintain capability to operate with the different MEMS chip.

$$V_o = \frac{V_b * dc}{C\text{int}} \tag{1}$$

The readout chain differential signal output from C/V go into the analog low pass filter, which can enables anti-alias filtering, and provides a reasonable buffered input signal to SDM.

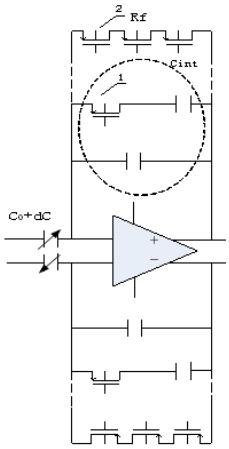

Fig.3 C/V converter working principle

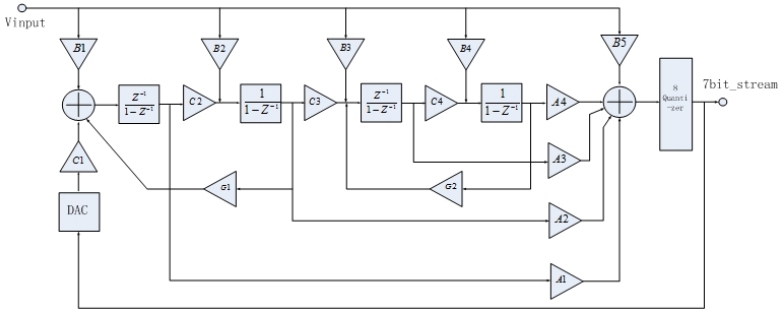

Fig.4 4th order CRFF module architecture

The design and implementation of sigma-delta modulator for capacitance detection and demodulation

The drive and sense loop,for the same signal delay, are actually the same differential channel capacitors detection, the one side of channel differential is shown in Fig.4, performs signal feedback control on the gyroscope MEMS capacitive drive or sense electrodes, and provides a digital output reading. The low-jitter exterior clock is the main clock of ASIC achieves better SNR for CT force-feedback operation. The loop is achieved by implementing a 4th-order low pass modulator using a *switch-capacitance* electronic filter. The modulator architecture is based on feed-forward topology with a feed-back branch to stabilize the loop. There are four typical structures for modulator, including CIFB (cascade-of-integrators with feed-back),CRFB (cascade-of-resonators with feed-back), CIFF (cascade-of-integrators with feed-forward) and CRFF (cascade-of-resonators with feed-forward) [2]. Among the four kinds of modulator structures, CRFF structure is adopted in this paper, the structure of 4th-order CRFF ADC is shown in Fig.4. When the modulator structure, modulator order, over sampling ratio, whether optimize zeros, the gain of pass-band, center frequency ,are fixed. The coefficients of the modulator are determined to be optimum through Matlab STD-Toolbox computation. The stability of modulator is decided by pole of NTF(Noise transfer function), and root locus of modulator is shown in Fig.5, to decide whether the modulator is stable. The root locus of the modulator indicates that the closed loop is stable as long as the quantization gain remains less than 0.699, as depicted in Fig.5.

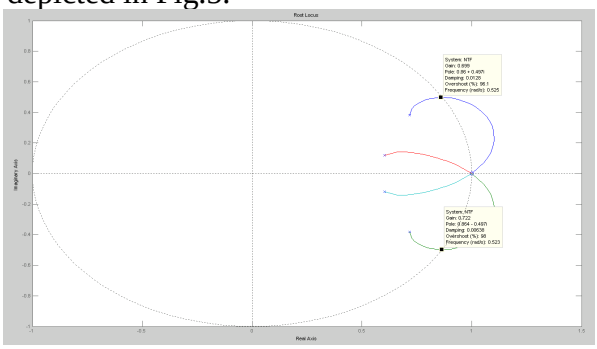

Fig.5 The root locus of the modulator

To attain an 20bit ENOB (effective number of bits), the ADC modulator is designed with an SNR of at least 120dB, and the capacitance ratios in 4 orders are matched accurately to realize the performance. Because of capacitor ratios for the g coefficients are not realizable, G1=G2=0, zero optimization is not be used. Considering the ADC modulator is implemented on CMOS technology. All the parameters of ADC modulator are shown in table I and modified by considering the value of switch capacitor.

Table 1 Coefficients of 4th-Order Sigma Delta ADC System

COEFFICIENTS	VALUE	MATCH CAPICITOR	REMARK
A1	0.8	$C_{forward2}$=1.0[pF], C_{sum}=1.25[pF]	
A2	0.6	$C_{forward3}$=0.75[pF], C_{sum}=1.25[pF]	$C_{forward3}$ Omit in Fig.5
A3	0.4	$C_{forward4}$=0. 5[pF], C_{sum}=1.25[pF]	$C_{forward4}$ Omit in Fig.6
A4	1.0	$C_{forward5}$=1. 25[pF], C_{sum}=1.25[pF]	$C_{forward5}$ Omit in Fig.6
C1	1.167	C_{input}=7[pF] , C_{f2}=6[pF]	
C2	0.5	C_3=0.5[pF], C_4=1.0[pF]	
C3	0.4	C_5=0.5[pF], C_6=1.25[pF]	Omit in Fig.6
C4	0.05	C_7=0.25[pF], C_8=5[pF]	Omit in Fig.6
B1	1.167	C_{input}=7[pF] , C_{f3}=6[pF]	C_{f3} Omit in Fig.6
B2	0	0	
B3	0	0	
B4	0	0	
B5	1.8	$C_{forward1}$=2.25[pF], C_{sum}=1.25[pF]	
G1	0	0	
G2	0	0	

Fig.6 shows an extract of the switched capacitor implementation of the modulator. There are some parts of electronic, for instance, although four integrators are embedded into the CRFF[3] modulator structures, the first and second integrators are shown in Fig. 6, the third and the fourth integrators are the same as the others and are omitted in Fig.6. VCMI is 1.65V as the common mode signal of the feedback part, that is compatibility the VCM is 0.9V as the common mode signal of the four integrators part.

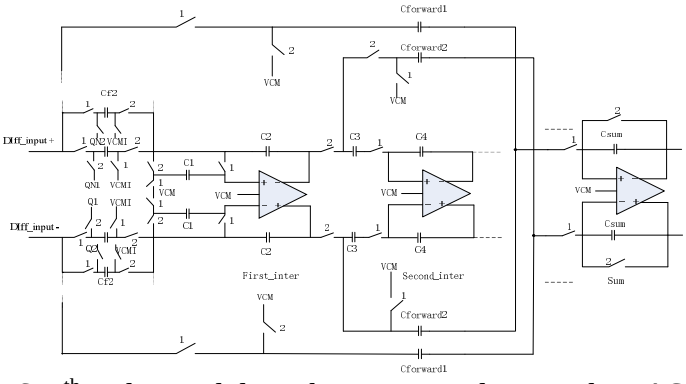

Fig.6 4th-order module architecture implemented on ASIC

In this paper, switched capacitor is the implement of the module architecture, as shown in Fig.7.While the first and third integrator sample their input signal in clock phase 1 and output valid signals at clock phase 2, the second and forth integrator operate in a reversed order. This is advantageous because additional sample and hold circuits would not been necessary. At this time sequence of switched capacitor, every the main clock can attain the sum of the 4 integrators, for go into the 8-level quantizer. The VREF is divided into 7 reference voltage generated by resistive voltage. The sum signal is compared with the 7 reference voltage by flash ADC with main clocked comparators to generate 7 lines thermometer code. The thermometer code is convenient for flash DAC feedback. For reducing the requirement of digital filter chain, The 7 lines thermometer code is converted into 3 bit binary code, which can reduce bus width from 7 to 3 without information loss. The 3 bit binary code is the output of the capacitance detection and beneficial to filter chain to deal with. Fig.8 is the ADC simulation results implement in ASIC, Fig.9 is the SNR and Power spectral density of ADC.

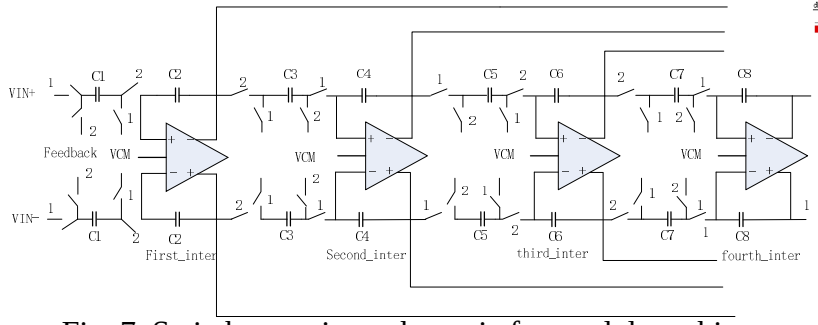

Fig. 7 Switch capacitor schematic for module architecture

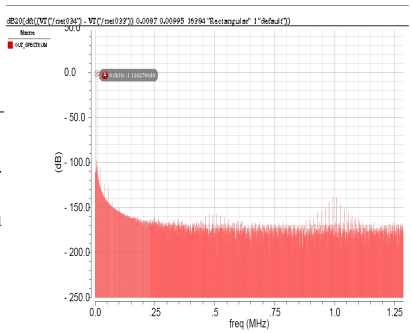

Fig.8 ADC simulation results

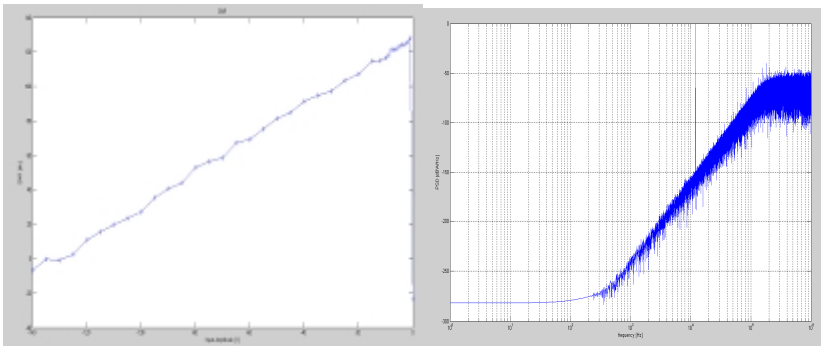

Fig.9 SNR vs input amplitude & Power spectral density of ADC

The filter chain and digital processing

The digital filters chain process the output bit-stream of the modulators of the drive and sense loops, and performs output demodulation, the demodulation output is decimated using a programmable decimation filter to change high rate 3bit-stream to low rate 24bit-stream. The filter chain is composed of a CIC [4] decimator filter, followed by a IIR band-pass filter, and a IIR band-stop filter, and a band-stop filter, and a CIC interpolator filter, finally a low-pass correction filter is used to compensate the non-flat frequency response of the CIC filter and the resonance signal in sense-loop. From the simulation the power spectrum result as presented in Fig.8, it can be seen that the SNR of the ADC modulator is over 120 dB, and can meet the precision requirement of the digitalized gyroscope system. Digital filter must also meet the precision requirement that SNR is over 120 dB. The CIC filter is designed in the digital part of the system to suppress the high frequency noise component[5]. The bit-stream with the sampling rate of 2MHz is generated from a module. The CIC filters are widely9 used in multi-sampling-rate processing systems, since fine filtering performance can be achieved through simple hardware structure, particularly suitable for FPGA and ASIC realization. The next filter is a “wide” band-pass to pass all possible drive frequencies from gyroscope. The band-pass is followed by a band-stop to suppress the sense-resonance in an effective way. Band-stop design guarantees zero points in the filter characteristic around this resonance frequency. And low-pass is implemented before the output that serves to suppress vibrations. Furthermore, it suppresses aliasing effects when the output rate of the interface is low. The CIC decimator and interpolator structures are shown in Fig.10.

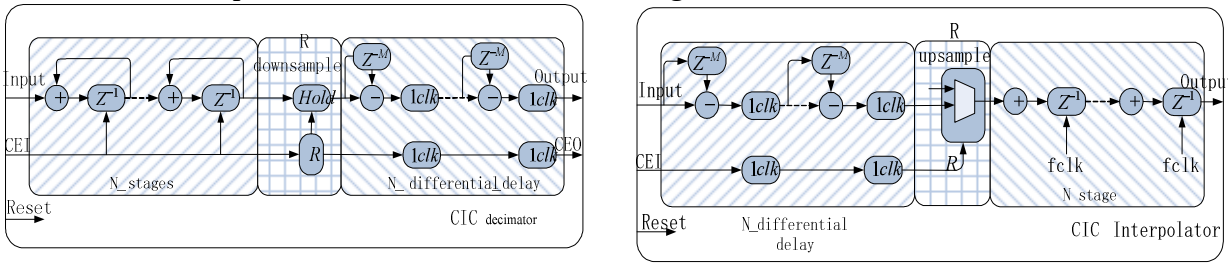

Fig.10 CIC decimator & Interpolator structure

As shown in Fig.11, The direct form II transposed is as a stage of IIR filter for a better filter implementing, and there are some reasons to prefer the transposed direct form II for the stages: The first is just only one common input of all A coefficient multipliers and all B coefficient multipliers,

The second is just only one multiplication operation to calculate next output from new input, The third is minimum count of storage elements, finally with implement two only multiply units and two add units there is a good balance between area and calculation time. At all it is the best way to implement a filter stage in an ASIC. The output and internal states are separated into four steps. Each step is controlled by a single step-signal and one control signal for the multipliers.

The SNR of oscillator frequency in band-pass is above the 125dB though the filter simulation, The suppressing of the sense-resonance is over 60dB, the filter design meet the requirement of the digital system of the gyroscope, and All the filter simulation results are shown in Fig.12-16.

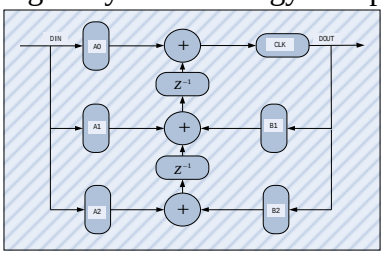

Fig.11 IIR filter stage

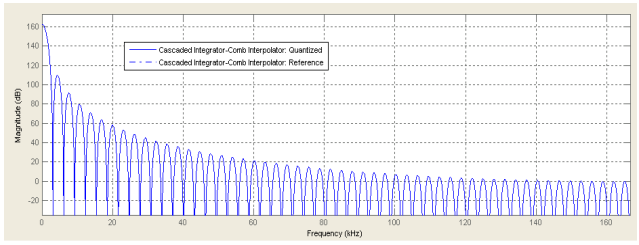

Fig.12 CIC interpolator simulation result

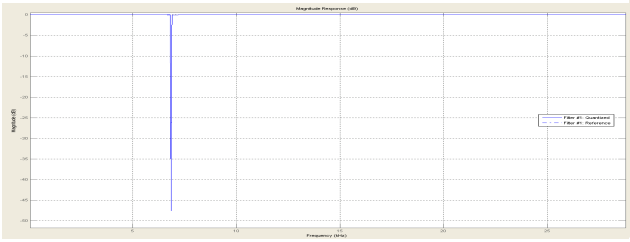

Fig.13 Band-stop simulation result

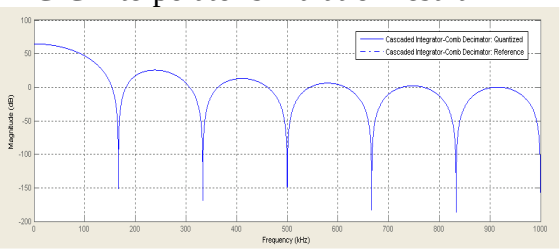

Fig.14 CIC decimator simulation result

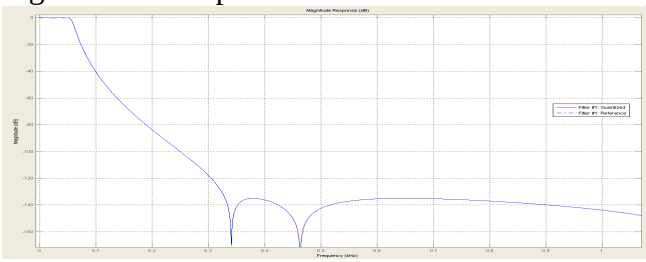

Fig.15 Low-pass simulation result

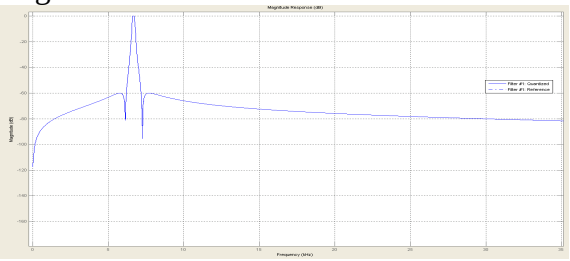

Fig.16 Band-pass simulation result

IMPLEMENTATION AND MEASURMENTS

This paper describes an ASIC interface for MEMS gyroscopes is including an analog ASIC and a digital ASIC[6], The ASICs are fabricated in 0.18um HVCMOS process, occupy $4\times3mm^2$, and dissipates 150mW in total from a single 5V, connected with gyroscope chip and each other with wire-bonding, The Analog ASIC packaged along with gyroscope chip in a single LTCC-48 packaging, The digital ASIC is sealing in the other single LTCC-48 packaging, The two LTCC-48 packagings are combined in a single printed board. The ASICs were tested with a MEMS gyroscope sensing element supplied by Micro-system. The measured DC transfer characteristics of the gyroscope is presented in Fig.18. The full-scale signal is ±500°/s .The output gyroscope noise floor and maximum linearity error measured can meet high performance gyroscope requirements.

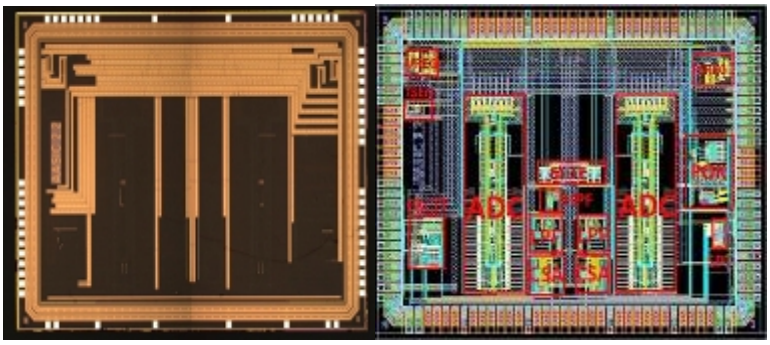

Fig.17 AASIC PHOTO & Function region

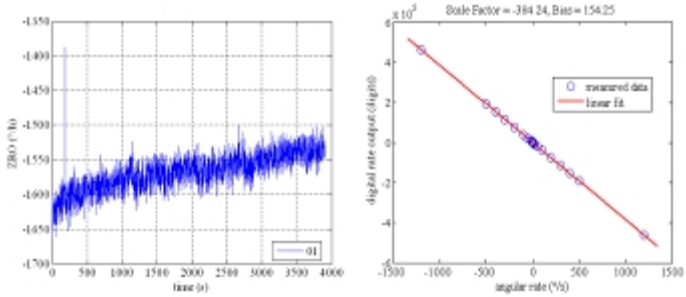

Fig.18 Gyroscope output &DC transfer characteristics (output digital vs. input angular velocity).

Conclusions

This paper describes an ASIC interface for MEMS gyroscope. The ASIC employs PLL to trace the drive frequency, PID to stable the drive amplitude. A 4th-order CRFF architecture low-pass sigma-delta-modulator and filter chain are used in drive-loop and sense-loop to achieve high level in gyroscope signal detection, which provides stable operation in harsh environments. The same signal channel can supply the precise demodulation phase. The ASICs provide a fully integrated solution with on-chip reference generation, power management, and temperature compensation, In addition to a complete digital filter chain solution for signal processing including CIC and IIR filters, ZRO cancellation, temperature compensation of both the scale factor and ZRO, and a standard serial interface channel containing even parity check. The digital core also generates a self-test signal that allows a fail-safe operation.

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References

[1] Saukoski M. *System and circuit design for a capacitive MEMS gyroscope*[D]. Espoo, Finland: Helsinki University of Technology, (2008): 15-18.

[2] A.N. Nordin and M. Zaghloul, "*CMOS design and implementation of sigma-delta analog-to-digital data converter suitable for MEMS devices*", (2003).

[3] Q. Fu, W. P. Chen, S. Chen, P. F. Wang, and X. W. Liu, "*A high bandwidth sigma-delta modulator applied in micro-gyroscope*",Key Eng.Mater., vols. 562–565, pp. 369–373, Jul. (2013).

[4] Jovanovic Dolecek and Fred Harris, "*Design of CIC Compensator Filter in a Digital IF Receiver*", (2008 IEEE).

[5] Gordana Jovanovic Dolecek and Fred Harris, "*On Design of Two- Stage CIC Compensation Filter*", IEEE International Symposium on Industrial Electronics, Seoul, Korea,pp. 903-908, July 5-8, (2009).

[6] J. C. Candy and G. C. Temes, *Oversampling Delta-Sigma Data Converters—Theory, Design and Simulation*. New York: IEEE Press,(1992).